APPLICATION		REVISION			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	C-65	1	ADVANCE ENGINEERING RELEASE	1/31/91	MA.

1.0 DESCRIPTION

This specification describes the requirements for a single chip 8- bit microcontroller unit fabricated in 2U CMOS double-metal technology for high speed and low power consumption. The IC is a fully static device that contains an enhanced 6502 microprocessor (65CE02), four independent 16-bit interval timers, two 24-hour (AM/PM) time of day clocks each with programmable alarm, full-duplex serial I/O (UART) channel with programmable baud rate generator, built-in memory map function to access up to 1 megabyte of memory, two 8-bit shift registers for synchronous serial I/O, and 27 individually programmable I/O lines.

1.1 CONFIGURATION

This IC device shall be configured in a standard, 84-pin plastic chip carrier package. Refer to figure 3.1 for package details

1.2 SOURCES

Refer to the Approved Vendor List

1.3 APPLICABLE DOCUMENTS

Commodore Engineering Policy 1.02.007
Commmodre Enginggering Policy 1.02.008
Commodore Specification 310072 rev B.
I.C. Qualification Procedure
OEM Environmental Requirements
I.C. Branding Requirements

COMMODORE P. N.	STATUS
390490-01	ACTIVE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/- 0.02
3 PLACE DECIMALS +/- 0.01

DRAWN
Mike Rivers

SYSTEM ENG.

TEST ENG

COMP. ENG
Drew Shannon

CIRCUIT ENG.

COPYRIGHT 1991
COMMODORE ELECTRONICS LTD
INFORMATION CONTAINED HEREIN IS THE UNPUBLISHED AND CONFIDENTIAL PROPERTY OF COMMODORE ELECTRONICS LIMITED. USE, REPRODUCTION OR DISCLOSURE OF THIS INFORMATION WITHOUT THE PRIOR WRITTEN PERMISSION OF COMMODORE IS STRICTLY PROHIBITED. ALL RIGHTS RESERVED.

Commodore
1200 WILSON DRIVE
WEST CHESTER, PA. 19380
(215) 431-9100

TITLE:
IC, LSI, MICROPROCESSOR, 4510

SIZE A | DRAWING NUMBER 390490

SCALE

2.0 PIN CONFIGURATION

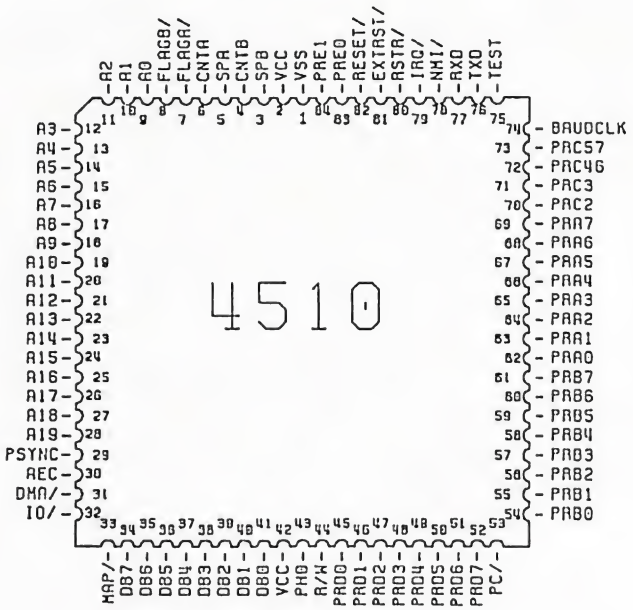

FIGURE 1
PIN CONFIGURATION
(refer to figure 6 for pin-name reassignment for C65 application)

2.1 BLOCK DIAGRAM

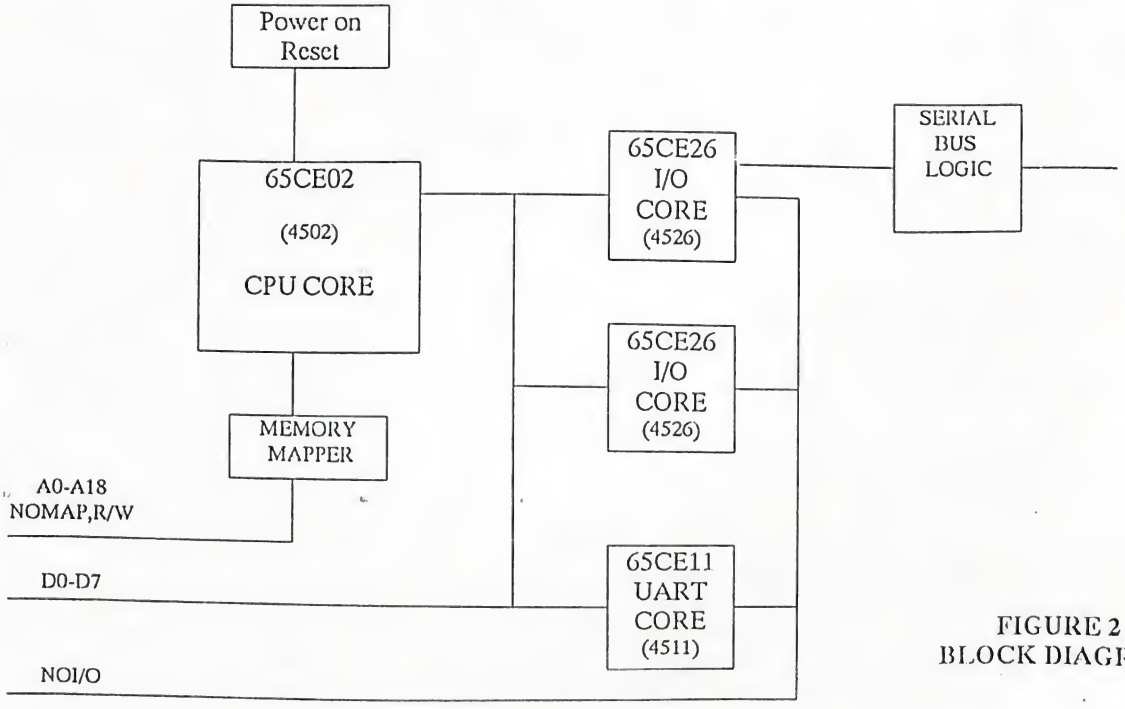

FIGURE 2
BLOCK DIAGRAM

Commodore	TITLE: IC, LSI, MICROPROCESSOR, 4510			
SIZE: A	DRAWING NUMBER: 390490	REV.: 1	SCALE:	SHEET 2 OF 52

2.0 FUNCTIONAL DESCRIPTION

2.1 PIN DESCRIPTION

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
VSS	1	IN	This is the power ground signal (0 volts)
VCC	2,42	IN	This is the power supply signal (+5 volts)
SPB, SPA	3 5	I/O I/O	The SPA and SPB signals are open-drain and bi-directional, each with a 3K ohm (min.) passive pull-up. The SPA and SPB signals are the data lines used by the two 8-bit synchronous serial port registers. In input mode, SPA and SPB are clocked into the device on the rising edge of the CNTA and CNTB clocks, respectively. In the output mode, SPA and SPB change on the falling edge of the CNTA and CNTB clocks, respectively.
CNTB CNTA	4 6	I/O I/O	The CNTA and CNTB signals are open-drain and bi-directional, each with a 3K ohm (min.) passive pull-up. These pins are internally synchronized to the PH0 clock and then used to clock the synchronous serial registers, in input mode. In output mode, each pin will reflect the clock signal derived from the corresponding timer.
FLAGA/ FLAGB/	7 8	I/O IN	The FLAGA/ and FLAGB/ inputs are negative edge sensitive input signals. A passive pull-up (3K ohm min) is tied on each of these pins. They are internally synchronized to the PH0 clock and are used as general purpose interrupt inputs. Any negative transition on either of these signals will cause the device to start an interrupt sequence, provided that the proper bit is set in each of the interrupt mask registers; the device will drop the IRQ/ line to indicate that an interrupt sequence is underway.

*** When the FAST SERIAL MODE is enabled ***
*** the CNTA, SPA and FLAGA/ lines will ***
*** not function as described above. See ***
*** section 2.5.6 for FAST SERIAL MODE ***
*** description ***

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
A0-A19	9 thru 28	I/O	Address Bus - This is a 20 bit bi-directional bus with tri-state outputs. The output of each address line is TTL compatible, capable of driving two standard TTL loads and 55 pf. When the DMA/ or AEC line goes low, this bus goes tri state. A0-A3, A8 andA9 select an internal I/O register. If AEC and DMA are high, the bus will be driven by the CPU.
PSYNC	29	OUT	This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The PSYNC line is high throughout the OP CODE fetch a cycle.
AEC	30	IN	This input signal is the Address Enable Control line. When high, the address bus, MAP/, and R/W are valid. When low, the address bus, R/W and MAP/ are in a high impedance state. If AEC is low when PH0 input falls, the CPU will halt for the current cycle.
DMA/	31	IN	This signal is connected to a 3K passive pull- up. When this signal is low the address bus , MAP/, and R/W will be tri-stated. This will allow external DMA devices to assume control of the system bus lines.

A low state on either DMA/ or AEC during the falling transition of phase zero (PH0) will halt the Microprocessor with the current output address, R/W, MAP/ and data. This feature allows external bus masters access to these busses.

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
IO/	32	IN	This input signal is used to select the internal registers of the device, provided MAP/ is high.
MAP/	33	I/O	This signal is passively pulled-up (3 Kohm) whenever DMA/ or AEC is pulled low. This output signal is used to indicate whether or not memory is being mapped by the device. If the CPU is addressing a mapped memory region the MAP/ line will go low and will inhibit the IO/ line from selecting an internal register. If the CPU is not mapping memory the MAP/ line will be high A16-A19 will be low for all unmapped accesses When /MAP and IO/ are both pulled low , (new TEST mode), the Data Bus pins will not be tri-stated when AEC or DMA/ goes low.
DB7-DB0	34 thru 41	I/O	D0-D7 form an 8 bit bi-directional data bus for data exchanges tbetween the internal CPU, registers, and external peripheral devices and memory. The output buffers are capable of driving two standard TTL loads and 55pf.
R/W	43	I/O	This signal is generated by the CPU to control the direction of data transfers on the data bus.This line is high except when the CPU is writing to memory, an internal I/O register or an external device. When the AEC or DMA/ signal is low, the R/W becomes tri-state.
PH0	44	IN	This clock is a TTL compatible input used for internal device operation and as a timing reference for communicating with the system data bus.
PC/	53	OUT	This output line is a strobe signal and is Centronics interface compatible. The signal goes low following a read or write access of PORT D.
PRD0-PRD7	45 thru 52	I/O	These are three 8-bit ports with each of their lines having a passive pull-up (min. 3K ohm) . Each individual port line may be programmed to be either input or output.
PRB0-PRB7	54 thru 61	I/O	
PRA0-PRA7	62 thru 69	I/O	Same as the PRD and PRB lines described above.

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
PRC2	70	I/O	This line corresponds to PORT C, bit 2. It has passive pull-up (min. 3k ohm). The line can be configured as input or output. PRC2 becomes the external shift register clock when the UART is configured to operate in the synchronous mode, otherwise PRC2 operates as normal.
PRC3	71	OUT	This signal is an open drain output with a passive pull-up (1K ohm min). It corresponds to bit 3 of PORT C. When this port bit is set as an input, the PRC3 line is driven low; reading the port bit will give a high. If configured as an output, reading this port bit will not givethe status of the PRC3 line but the value previously written on the PORT C data reg. bit 3.
PRC46	72	I/O	This is an open drain bi-directional signal with a passive pull-up (1K ohm min). Bit 6 of PORT C is always configured as an input; the bit will give the status of the PRC46 line anytime the port is read, regardless of what is written in the data direction register. If bit 4 of PORT C, PC4 ,is set as an input, the PRC46 line will be pulled low; reading the port bit will give a high. If bit 4 is configured as an output, PRC46 will be pulled low if bit 4 in the port data register is high, otherwise the PRC46 line will float to a high.
PRC57	73	I/O	This is an open drain bi-directional signal with a passive pull-up (1K ohm min). Bit 7 of PORT C is always configured as an input; the bit will give the status of the PRC57 line anytime the port is read, regardless of what is written in the data direction register. If bit 5 of PORT C, PC5, is set as an input, the PRC57 line will be pulled low; reading the port bit will give a high. If bit 5 is configured as an output, PRC57 will be pulled low if bit 5 in the port data register is high, otherwise thePRC57 line will float to a high.

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
PRE0,PRE1	83, 84	I/O	This a 2-bit port with each line having a passive pull-up (min. 3K ohm) as well as active pull-up and pull-down transistors. Each individual port line may be programmed to be either input or output.
BAUDCLK	74	IN	This input is a 7MHz clock used to drive the UART Baud Rate Generator, and is assumed to be synchronous with the PH0 clock. This clock is also divided down to 1MHz to drive the interval timers, and down to 10Hz to drive the TOD timers. This clock is also used to time out the POR and RESTORE (RSTR*) circuits.
TEST	75	IN	When this input goes to a high state, the device will operate in a test mode. The test mode will allow the BAUDCLK dividers to be initialized and the TOD and interval timers to be driven directly by the BAUDCLK clock, bypassing all the dividers.
TXD	76	OUT	This is the UART transmit data output line. The LSB of the Transmit Data Register is the first data bit transmitted. The data transmission rate (baud rate) is determined by the value written to the Baud Rate Timer latches.
RXD	77	IN	This is the UART receive data input line. The first data bit received is loaded into theLSB of the Receive Data Register. The receiver data rate must be the same as that determined by the value written to the Baud Rate Timer latches
NMI/	78	I/O	The NMI/ pin is an open drain bi-directional signal. A passive pull-up (3K ohms minimum) is tied on this pin, allowing multiple NMI/ sources to be tied together. A negative transition on this pin requests a non-maskable interrupt sequence to be generated by the microprocessor. The interrupt sequence will begin with the first PSYNC after a multiple-cycle opcode. NMI/ inputs cannot be masked by the processor status register I flag. The two program counter bytes PCH and PCL, and the processor status register P, are pushed onto the stack. Then the program counter bytes PCL and PCH are loaded from memory addresses FFFA and FFFB, respectively.

NOTE: Since this interrupt is non-maskable, another NMI/ can occur before the first is finished. Care should be taken to avoid this.The NMI/ line is normally off (high impedance) and the device will activate it low as described in the functional description. AEC and DMA/ must be high for any interrupt to be recognized. All interrupts (including NMI/ are inhibited following execution of a MAP/ opcode. Interrupts are re-enabled by executing a NOP opcode.

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
IRQ/	79	I/O	The Interrupt Request line (IRQ/) is an open drain bi-directional signal. A passive pull-up (3KΩ minimum) is tied on this pin, allowing multiple IRQ/ sources to be connected together. This pin is sampled during PH2 and when a negative transition is detected an interrupt will be activated, only if the mask flag(I) in the status register is low. The interrupt sequence will begin with the first PSYNC after a multiple-cycle opcode. The two program counter bytes PCH and PCL, and the processor status register P, are stored onto the stack; the interrupt mask flag is set high so that no further IRQ/'s may occur. At the end of this cycle, the program counter low byte (PCL) will be loaded from address FFFE, and the high byte (PCH) from FFFF, thus transferring program control to the vector located at these addresses. The IRQ/ line is normally off (high impedance) and the device will activate it low as described in the functional description. AEC and DMA/ must be high for any interrupt to be recognized.

NOTE: Since this interrupt is non-maskable, another NMI/ can occur before the first is finished. Care should be taken to avoid this.The NMI/ line is normally off (high impedance) and the device will activate it low as described in the functional description. AEC and DMA/ must be high for any interrupt to be recognized. All interrupts (including NMI/ are inhibited following execution of a MAP/ opcode. Interrupts are re-enabled by executing a NOP opcode.

RESTR/	80	IN	This input is tied to a 3KΩ (min.) passivepull-up. A bounce eliminator circuit is used on this pin to remove any bounce during its falling transition, if the pin is tied to a contact closure. If the device sees a negative transition on this pin, it will immediately assert the NMI/ line to start a Non-Maskable Interrupt sequence. The device will ignore any subsequent transitions on the RESTR/ line until 4.2ms has elapsed, at which time the NMI/ line is de-asserted.
EXTRST/	81	OUT	This output is an open drain output with a min.1KΩ pull-up. This pin is asserted during power-up, and will stay low until 0.9 seconds after VDD has reached its operating voltage (assuming a 7MHz baud clock is present).

PIN NAME	SIGNAL NUMBER	DIRECTION	DESCRIPTION
RESET/	82	I/O	The Reset line (RESET/) is an open drain bidirectional signal. A passive pull-up (1KΩ minimum) is tied on this pin, allowing any external source to initialize the device. A low on RESET/ will instantly initialize the internal 65CE02 and all internal registers. All port pins are set as inputs and port registers to zero (a read of the ports will return all highs because of passive pull-ups); all timer control registers are set to zero and all timer latches to ones. All other registers are reset to zero (assuming a 7MHz baud clock is present). During power-up RESET/ is held low and will go high 0.9 seconds after VDD reaches the operating voltage. If pulled low during operation, the currently executing opcode will be terminated. The B and Z registers will be cleared. The stack pointer will be set to "byte" mode, with the stack page set to page 1. The processor status bits E and I will be set. When the high transition is detected, the reset sequence begins on the CPU cycle. The first four cycles of the reset sequence do nothing. Then the program counter bytes PCL and PCH are loaded from memory addresses FFFC and FFFD, and normal program execution begins.

2.2 REGISTER ADDRESS ALLOCATION

This device contains a total of 42 I/O peripheral registers which can be accessed after the following conditions are met. In an access cycle, the device must be in a non-mapped mode (MAP/ line is not asserted), the IO/ line must be in an active low state and the A0-A3, A8 and A9 address lines must contain the valid address of the register to be accessed. In addition, the state of the R/W line will indicate whether a read (R/W is "high") or a write (R/W is "low") cycle is under way.

A9	A8------ A3	A2	A1	A0	HEX ADD	REG SYMBOL	REGISTER NAME
0	0 0	0	0	0	0X0	PRA	Peripheral Data Reg A
0	0 0	0	1	0	0X1	PRB	Peripheral Data Reg B
0	0 0	1	0	1	0X2	DDRA	Data Direction Reg A
0	0 0	0	1	1	0X3	DDRB	Data Direction Reg B
0	0 0	1	0	0	0X4	TA LO	Timer A Low Register
0	0 0	1	0	1	0X5	TA HI	Timer A High Register
0	0 0	1	1	0	0X6	TB LO	Timer B Low Register
0	0 0	1	1	1	0X7	TB HI	Timer B High Register
0	0 1	0	0	0	0X8	TODATS	TODA 10ths Sec Register
0	0 1	0	0	1	0X9	ODAS	TODA Seconds Register
0	0 0	1	1	0	0XA	TODAM	TODA Minutes Register
0	0 1	0	1	1	0XB	TODAH	TODA Hours-AM/PM Reg
0	0 1	1	0	0	0XC	SDRA	SERIALA Data Register
0	0 1	1	0	1	0XD	ICRA	INTERRUPTA Control Reg.
0	0 1	1	1	0	0XE	CRA	Control Register A
0	0 1	1	1	1	0XF	CRB	Control Register B
0	1 0	0	0	0	1X0	PRC	Peripheral Data Reg C
0	1 0	0	1	1	1X1	PRD	Peripheral Data Reg D

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX ADD	REG SYMBOL	REGISTER NAME
0	1	0	0	1	0					1X2	DDRC	Data Direction Reg C
0	1	0	0	1	1					1X3	DDRD	Data Direction Reg D
0	1	0	1	0	0					1X4	TC LO	Timer C Low Register
0	1	0	1	0	1					1X5	TC HI	Timer C High Register
0	1	0	1	1	0					1X6	TD LO	Timer D Low Register
0	1	0	1	1	1					1X7	TD HI	Timer D High Register
0	1	1	0	0	0					1X8	TODBTS	TODB 10ths of Sec Reg
0	1	1	0	0	1					1X9	TODBS	TODB Seconds Register
0	1	1	0	1	0					1XA	TODBM	TODB Minutes Register
0	1	1	0	1	1					1XB	TODBH	TODB Hours-AM/PM Reg.
0	1	1	1	0	0					1XC	SDRB	SERIALB Data Register
0	1	1	1	0	1					1XD	ICRB	INTERRUPTB Control Reg.
0	1	1	1	1	0					1XE	CRC	Control Register C
0	1	1	1	1	1					1XF	CRD	Control Register D
1	0	0	0	0	0					2X0	DRE	Receive/Transmit Data Reg
1	0	0	0	0	1					2X1	URSR	UART Status Register
1	0	0	0	1	0					2X2	URCR	UART Control Register
1	0	0	0	1	1					2X3	BRLO	Baud Rate Timer LO Reg.
1	0	0	1	0	0					2X4	BRHI	Baud Rate Timer HI Reg.
1	0	0	1	0	1					2X5	URIENB	UART Irq Enable Reg.
1	0	0	0	0	0					2X0	DREG	Receive/Transmit Data Reg.
1	0	0	0	0	0					2X1	URSR	UART Status Register
1	0	0	0	1	0					2X2	URCR	UART Control Register
1	0	0	0	1	1					2X3	BRLO	Baud Rate Timer LO Reg.
1	0	0	1	0	0					2X4	BRHI	Baud Rate Timer HI Reg.
1	0	0	1	0	1					2X5	URIEN	UART IRQ Enable Reg.
1	0	0	1	1	0					2X6	URIFG	UART Irq Flag Reg.
1	0	0	1	1	1					2X7	PRE	Peripheral Data Reg. E
1	0	1	0	0	0					2X8	DDRE	Data Direction E
1	0	1	0	0	1					2X9	FSREG	FAST SERIAL Register

READ/ WRITE	REG	NAME		D7	D6	D5	D4	D3	D2	D1	D0
R/W	0X0	PRA		PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	0X1	PRB		PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	0X2	DDRA		DPA7	DPA6	DPA5	DPA4	DPA3	DPA2	DPA1	DPA0
R/W	0X3	DDRB		DPB7	DPB6	DPB5	DPB4	DPB3	DPB2	DPB1	DPB0
READ	0X4	TA LO	TIMER	TAL7	TAL6	TAL5	TAL4	TAL3	TAL2	TAL1	TAL0
READ	0X5	TA HI	TIMER	TAH7	TAH6	TAH5	TAH4	TAH3	TAH2	TAH1	TAH0
READ	0X6	TB LO	TIMER	TBL7	TBL6	TBL5	TBL4	TBL3	TBL2	TBL1	TBL0
READ	0X7	TB HI	TIMER	TBH7	TBH6	TBH5	TBH4	TBH3	TBH2	TBH1	TBH0
WRITE	0X4	TA LO	PRESCALER	PAL7	PAL6	PAL5	PAL4	PAL3	PAL2	PAL1	PAL0
WRITE	0X5	TA HI	PRESCALER	PAH7	PAH6	PAH5	PAH4	PAH3	PAH2	PAH1	PAH0
WRITE	0X6	TB LO	PRESCALER	PBL7	PBL6	PBL5	PBL4	PBL3	PBL2	PBL1	PBL0
WRITE	0X7	TB HI	PRESCALER	PBH7	PBH6	PBH5	PBH4	PBH3	PBH2	PBH1	PBH0
READ	0X8	TODATS	TOD TIMER	0	0	0	0	TA8	TA4	TA2	TA1
READ	0X9	TODAS	TOD TIMER	(*) 0	SAH4	SAH2	SAH1	SAL8	SAL4	SAL2	SAL1
READ	0XA	TODAM	TOD TIMER	(*) 0	MAH4	MAH2	MAH1	MAL8	MAL4	MAL2	MAL1
READ	0XB	TODAH	TOD TIMER	APM	0	0	HAH	HAL8	HAL4	HAL2	HAL1
				(*) IN TEST MODE: WILL READ DIVIDER STAGE OUTPUTS							
WRITE	0X8	TODATS	TOD LATCHES	0	0	0	0	TA8	TA4	TA2	TA1
WRITE	0X9	TODAS	TOD LATCHES	0	SAH4	SAH2	SAH1	SAL8	SAL4	SAL2	SAL1
WRITE	0XA	TODAM	TOD LATCHES	0	MAH4	MAH2	MAH1	MAL8	MAL4	MAL2	MAL1
WRITE	0XB	TODAH	TOD LATCHES	APM	0	0	HAH	HAL8	HAL4	HAL2	HAL1
				IF CRB ALARM BIT=1 , ALARM REGISTER IS WRITTEN IF CRB ALARM BIT=0 , TOD REGISTER IS WRITTEN							

TABLE 1
REGISTER BIT ALLOCATION

READ/ WRITE	REG	NAME		D7	D6	D5	D4	D3	D2	D1	D0
R/W	0XC	SDRA		SRA7	SRA6	SRA5	SRA4	SRA3	SRA2	SRA1	SRA0
READ	0XD	ICRA (INT DATA)		IRA	0	0	FLGA	SPA	ALRMA	TB	TA
WRITE	0XD	ICRA (INT MASK)		AS/$\overline{C}$	--	--	FLGA	SPA	ALRMA	TB	TA
R/W	0XE	CRA		TODA IN	SPA MODE	TMRA INMODE	LOADA	RUN-A MODE	OUT-A MODE	PRB6 ON	STARTA
R/W	0XF	CRB		ALARM (TODA)	TIMERB CRB6	INMODE CRB5	LOADB	RUN-B MODE	OUT-B MODE	PRB7 ON	STARTB
READ	1X0	PRC		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	1X1	PRD		PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	1X2	DDRC		DPC7	DPC6	DPC5	DPC4	DPC3	DPC2	DPC1	DPC0
R/W	1X3	DDRD		DPD7	DPD6	DPD5	DPD4	DPD3	DPD2	DPD1	DPD0
READ	1X4	TC LO	TIMER	TCL7	TCL6	TCL5	TCL4	TCL3	TCL2	TCL1	TCL0
READ	1X5	TC HI	TIMER	TCH7	TCH6	TCH5	TCH4	TCH3	TCH2	TCH1	TCH0
READ	1X6	TD LO	TIMER	TDL7	TDL6	TDL5	TDL4	TDL3	TDL2	TDL1	TDL0
READ	1X7	TD HI	TIMER	TDH7	TDH6	TDH5	TDH4	TDH3	TDH2	TDH1	TDH0
WRITE	1X4	TC LO	PRESCALER	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
WRITE	1X5	TC HI	PRESCALER	PCH7	PCH6	PCH5	PCH4	PCH3	PCH2	PCH1	PCH0
WRITE	1X6	TD LO	PRESCALER	PDL7	PDL6	PDL5	PDL4	PDL3	PDL2	PDL1	PDL0
WRITE	1X7	TD HI	PRESCALER	PDH7	PDH6	PDH5	PDH4	PDH3	PDH2	PDH1	PDH0
READ	1X8	TODBTS	TOD TIMER	0	0	0	0	TB8	TB4	TB2	TB1
READ	1X9	TODBS	TOD TIMER	(*) 0	SBH4	SBH2	SBH1	SBL8	SBL4	SBL2	SBL1
READ	1XA	TODBM	TOD TIMER	0	MBH4	MBH2	MBH1	MBL8	MBL4	MBL2	MBL1
READ	1XB	TODBH	TOD TIMER	BPM	0	0	HBH	HBL8	HBL4	HBL2	HBL1
				(*) IN TEST MODE: WILL READ DIVIDER STAGE OUTPUT							

REGITER BIT ALLOCATION

READ/ WRITE	REG	NAME	D7	D6	D5	D4	D3	D2	D1	D0
WRITE	1X8	TODBTS (TOD LATCHES)	0	0	0	0	TB8	TB4	TB2	TB1
WRITE	1X9	TODBS	0	SBH4	SBH2	SBH1	SBL8	SBL4	SBL2	SBL1
WRITE	1XA	TODBM	0	MBH4	MBH2	MBH1	MBL8	MBL4	MBL2	MBL1
WRITE	1XB	TODBH	BPM	0	0	HBH	HBL8	HBL4	HBL2	HBL1
			IF CRD ALARM BIT=1 , ALARM REGISTER IS WRITTEN IF CRD ALARM BIT=0 , TOD REGISTER IS WRITTEN							
R/W	1XC	SDRB	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
READ	1XD	ICRB (INT DATA)	IRB	0	0	FLGB	SPB	ALRMB	TD	TC
WRITE	1XD	ICRB (INT MASK)	BS/C¯	--	--	FLGB	SPB	ALRMB	TD	TC
R/W	1XE	CRC	TODB IN	SPB MODE	TMRC INMODE	LOADC	RUN-C MODE	OUT-C MODE	PRD6 ON	STARTC
R/W	1XF	CRD	ALARM (TODB)	TIMERD CRD6	INMODE CRD5	LOADD	RUN-D MODE	OUT-D MODE	PRD7 ON	STARTD
READ (RECEIVE DATA REG)	2X0	DREG	RCV7	RCV6	RCV5	RCV4	RCV3	RCV2	RCV1	RCV0
WRITE (TRANSMIT DATA REG)	2X0	DREG	XMT7	XMT6	XMT5	XMT4	XMT3	XMT2	XMT1	XMT0
READ	2X1	URSR	TDONE	TEMPTY	ENDT	IDLE	FRME	PRTY	OVR	RFULL
WRITE	2X1	URSR	--	--	ENDT	IDLE	--	--	--	--
R/W	2X2	URCR	XMITR EN	RCVER EN	UART UM1	MODE UM0	CHAR CH1	LENGTH CH0	PARITY EN	PARITY EVEN
R/W	2X3	BRLO	BRL7	BRL6	BRL5	BRL4	BRL3	BRL2	BRL1	BRL0
R/W	2X4	BRHI	BRH7	BRH6	BRH5	BRH4	BRH3	BRH2	BRH1	BRH0
R/W	2X5	URIEN	XMTR IRQEN	RCVR IRQEN	XMTR NMIEN	RCVR NMIEN	-- --	-- --	-- --	-- --
READ	2X6	URIFG	XMTFLG	RCVFLG	--	--	--	--	--	--
R/W	2X7	PRE	--	--	--	--	--	--	PE1	PE0
R/W	2X8	DDRE	--	--	--	--	--	--	DPE1	DPE0
R/W	2X9	FSREG	DMODE*	FSDIR*	--	--	--	--	--	--

REGITER BIT ALLOCATION

Commodore

TITLE: IC, LSI, MICROPROCESSOR, 4510

SIZE	DRAWING NUMBER	REV.	SCALE	SHEET 13 OF 52
	399490	1		

2.4 CPU OPERATION

2.4.1 65CE02 Registers

The 65CE02 has the following 8 user registers.

A	accumulator
X	index-X
Y	index-Y
Z	index-Z
B	Base-page
P	Processor status
SP	Stack pointer
PC	Program counter

Accumulator
The accumulator is the only general purpose computational register. It can be used for arithmetic functions add, subtract, shift, rotate, negate, and for Boolean functions and, or, exclusive-or, and bit operations. It cannot, however, be used as an index register.

Index X
The index register X has the largest number of opcodes pertaining to, or using it. It can be incremented, decremented, or compared, but not used for arithmetic or logical (Boolean) operations. It differs from other index registers in that it is the only register that can be used in indexed-indirect or (bp,X) operations. It cannot be used in indirect-indexed or (bp), X mode.

Index Y
The index register Y has the same computational constraints as the X register, but finds itself in a lot less of the opcodes, making it less generally used. But the index Y has one advantage over index X, in that it can be used in indirect-indexed operations or (bp),Y mode.

Index Z
The index register Z is the most unique, in that it is used in the smallest number of opcodes. It also has the same computation limitations as the X and Y registers, but has an extra feature. Upon reset, the Z register is cleared so that the STZ (store zero) opcodes and non-indexed indirect opcodes from previous 65C02 designs are emulated. The Z register can also be used in indirect-indexed or (bp),Z operations.

Base page B register
Early versions of 6502 microprocessors had a special subset of instructions that required less code and less time to execute. These were referred to as the "zero page" instructions. Since the addressing page was always known, and known to be zero, addresses could be specified as a single byte, instead of two bytes.

The 65CE02 core also implements this same "zero page" set of instructions, but goes one step further by allowing the programmer to specify which page is to be the "zero page". Now that the programmer can program this page, it is now, not necessarily page zero, but instead, the "selected page". The term "base page" is used, however.

The B register selects which page will be the "base page", and the user sets it by transferring the contents of the accumulator to it. At reset, the B register is cleared, giving initially a true "zero page".

Processor status P register

The processor status register is an 8-bit register which is used to indicate the status of the microprocessor. It contains 8 processor "flags". Some of the flags are set or reset based on the results of various types of operations. Others are more specific.

The flags are...

Flag	Name	Typical indication
N	Negative	result of operation is negative
V	Overflow	result of add or subtract causes signed overflow
E	Extend	disables stack pointer extension
B	Break	interrupt was caused by BRK opcode
D	Decimal	perform add/subtract using BCD math
I	Interrupt	disable IRQ interrupts
Z	Zero	result of operation is zero
C	Carry	operation caused a carry

Stack Pointer SP

The stack pointer is a 16 bit register that has two modes. It can be programmed to be either an 8-bit page programmable pointer, or a full 16-bit pointer. The processor status E bit selects which mode will be used. When set, the E bit selects the 8-bit mode. When reset, the E bit selects the 16-bit mode.

Upon reset, the 65CE02 will come up in the 8-bit page-programmable mode, with the stack page set to 1. This makes it compatible with earlier 6502 products. The programmer can quickly change the default stack page by loading the Y register with the desired page and transferring its contents to the stack pointer high byte, using the TYS opcode. The 8-bit stack pointer can be set by loading the X register with the desired value, and transferring its contents to the stack pointer low byte, using the TXS opcode.

To select the 16-bit stack pointer mode, the user must execute a CLE (for CLear Extend disable) opcode. Setting the 16-bit pointer is done by loading the X and Y registers with the desired stack pointer low and high bytes, respectively, and then transferring their contents to the stack pointer using TXS and TYS. To return to 8-bit page mode, simply execute a SEE (SEt Extend disable) opcode.

```
*********************************************************** * *
*                        WARNING                              *
*                                                             *
*      If you are using Non-Maskable-Interrupts, or Interrupt *
*      Request is enabled, and you want to change BOTH stack  *
*      pointer bytes, do not put any code between the TXS and  *
*      TYS opcodes. Taking this precaution will prevent any    *
*      interrupts from occuring between the setting of the two *
*      stack pointer bytes, causing a potential for writing    *
*      stack data to an unwanted area.                         *
*********************************************************
```

Program Counter PC

The program counter is a 16-bit up-only counter that determines what area of memory that program information will be fetched from. The user generally only modifies it using jumps, branches, subroutine calls, or returns. It is set initially, and by interrupts, from vectors at memory addresses FFFA through FFFF (hex). See "Interrupts" below.

2.4.2 65CE02 Core Interrupts

There are three basic interrupt sources with the 65CE02 core. These are RES*, IRQ*, and NMI*, for Reset, Interrupt Request, and Non-Maskable Interrupt, and Set Overflow. The Reset is a hard non-recoverable interrupt that stops everything. The IRQ is a "maskable" interrupt, in that its occurance can be prevented. The NMI is "non-maskable", and if such an event occurs, can only be inhibited with the MAP opcode.

One important design feature, which must be remembered is that no interrupt can occur immediately after a one-cycle opcode. This is very important, because there are times when you want to temporarily prevent interrupts from occurring. The best example of this is, when setting a 16-bit stack pointer, you do not want an interrupt to occur between the times you set the low-order byte, and the high-order byte. If it could happen, the interrupt would do stack writes using a pointer that was only partially set, thus, writing to an unwanted area.After executing a MAP opode, all interrupts except RES* are inhibited until the execution of a NOP opcode.

IRQ*
The IRQ* (Interrupt ReQuest) input will cause an interrupt, if it is at a low logic level, and the I processor status flag is reset. The interrupt sequence will begin with the first SYNC after a multiple-cycle opcode. The two program counter bytes PCH and PCL, and the processor status register P, are pushed onto the stack. (This causes the stack pointer SP to be decremented by 3.) Then the program counter bytes PCL and PCH are loaded from memory addresses FFFE and FFFF, respectively.

An interrupt caused by the IRQ* input, is similar to the BRK opcode, but differs, as follows. The program counter value stored on the stack points to the opcode that would have been executed, had the interrupt not occurred. On return from interrupt, the processor will return to that opcode. Also, when the P register is pushed onto the stack, the B or "break" flag pushed, is zero, to indicate that the interrupt was not software generated.

NMI*
The NMI* (Non-Maskable Interrupt) input will cause an interrupt after receiving a high to low transition The interrupt sequence will begin with the first SYNC after a multiple-cycle opcode. NMI* inputs cannot be masked by the processor status register I flag. The two program counter bytes PCH and PCL, and the processor status register P, are pushed onto the stack. (This causes the stack pointer SP to be decremented by 3.) Then the program counter bytes PCL and PCH are loaded from memory addresses FFFA and FFFB.

As with IRQ*, when the P register is pushed onto the stack, the B or "break" flag pushed, and is zero, to indicate that the interrupt was not software generated.

RES*
The RES* (reset) input will cause a hard reset instantly as it is brought to a low logic level. This effects the following conditions. The currently executing opcode will be terminated. The B and Z registers will be cleared. The stack pointer will be set to "byte" mode, with the stack page set to page 1. The processor status bits E and I will be set.

The RES* input should be held low for at least 2 clock cycles. But once brought high, the reset sequence begins. The first four cycles of the reset sequence do nothing. Then the program counter bytes PCL and PCH are loaded from memory addresses FFFC and FFFD, and normal program execution begins.

2.4.3 65CE02 Core Addressing Modes

It should be noted that all 8-bit addresses are referred to as "byte" addresses, and all 16-bit addresses are referred to as "word" addresses. In all word addresses, the low-order byte of the address is fetched from the lower of two consecutive memory addresses, and the high-order byte of the address is fetched the higher of the two. So, in all operations, the low-order address byte is fetched first.

Implied OPR
The register or flag affected is identified entirely by the opcode in this (usually) single cycle instruction. In this document, any implied operation, where the implied register is not explicitly declared, implies the accumulator. Example: INC with no arguments implies "increment the accumulator".

Immediate (byte, word) OPR #xx
The data used in the operation is taken from the byte or bytes immediately following the opcode in the 2-byte or 3-byte instruction.

Base Page OPR bp (formerly Zero Page)
The second byte of the typically two-byte instruction contains the low-order address byte, and the B register contains the high-order address byte of the memory location to be used by the operation.

Base Page, indexed by X OPR bp,X (formerly Zero Page,X)
The second byte of the two-byte instruction is added to the X index register to form the low-order address byte, and the B register contains the high-order address byte of the memory location to be used by the operation.

Base Page, indexed by Y OPR bp,Y (formerly Zero Page,Y)
The second byte of the two-byte instruction is added to the Y index register to form the low-order address byte, and the B register contains the high-order address byte of the memory location to be used by the operation.

Absolute OPR abs
The second and third bytes of the three-byte instruction contain the low-order and high-order address bytes, respectively, of the memory location to be used by the operation.

Absolute, indexed by X OPR abs,X
The second and third bytes of the three-byte instruction are added to the unsigned contents of the X index register to form the low-order and high-order address bytes, respectively, of the memory location to be used by the operation.

Absolute, indexed by Y OPR abs,Y
The second and third bytes of the three-byte instruction are added to the unsigned contents of the Y index register to form the low-order and high-order address bytes, respectively, of the memory location to be used by the operation.

Indirect (word) OPR (abs)
The second and third bytes of the three-byte instruction contain the low-order and high-order address bytes, respectively, of two memory locations containing the low-order and high-order addresses, respectively.

Indexed by X, indirect (byte) OPR (bp,X) (formerly (zp,X))
The second byte of the two-byte instruction is added to the contents of the X register to form the low-order address byte, and the contents of the B register contains the high-order address byte, of two memory locations that contain the low-order and high-order address of the memory location to be used by the operation.

Indexed by X, indirect (word) OPR (abs,X)
The second and third bytes of the three-byte instruction are added to the unsigned contents of the X index register to form the low-order and high-order address bytes, respectively, of two memory locations containing the low-order and high-order address bytes.

Indirect, indexed by Y OPR (bp),Y (formerly (zp),Y)
The second byte of the two-byte instruction contains the low-order byte, and the B register contains the high-order address byte of two memory locations whose contents are added to the unsigned Y index register to form the address of the memory location to be used by the operation.

Indirect, indexed by Z OPR (bp),Z (formerly (zp))
The second byte of the two-byte instruction contains the low-order byte, and the B register contains the high-order address byte of two memory locations whose contents are added to the unsigned Z index register to form the address of the memory location to be used by the operation.

Stack Pointer Indirect, indexed by Y OPR (d,SP),Y
The second byte of the two-byte instruction contains an unsigned offset value, d, which is added to the stack pointer (word) to form the address of two memory locations whose contents are added to the unsigned Y register to form the address of the memory location to be used by the operation.

Relative (byte) Bxx LABEL
The second byte of the two-byte branch instruction is sign-extended to a full word and added to the program counter (now containing the opcode address plus two). If the condition of the branch is true, the sum is stored back into the program counter.

Relative (word) Bxx LABEL (branches only)
The second and third bytes of the three-byte branch instruction are added to the low-order and high-order program counter bytes, respectively. (the program counter now contains the opcode address plus two). If the condition of the branch is true, the sum is stored back into the program counter.

2.4.4 65CE02 Core Instruction Set

Add memory to accumulator with carry ADC

A=A+M+C

Addressing Mode	Abbrev.	Opcode
immediate	IMM	69
base page	BP	65
base page indexed X	BP,X	75
absolute	ABS	6D
absolute indexed X	ABS,X	7D
absolute indexed Y	ABS,Y	79
base page indexed indirect X	(BP,X)	61
base page indirect indexed Y	(BP),Y	71
base page indirect indexed Z	(BP),Z	72

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

The ADC instructions add data fetched from memory and carry to the contents of the accumulator. The results of the add are then stored in the accumulator. If the "D" or Decimal Mode flag is set, in the processor status register, then a Binary Coded Decimal (BCD) add is performed.

The "N" or Negative flag will be set if the sum is negative, otherwise it is cleared. The "V" or Overflow flag will be set if the sign of the sum is different from the sign of both addends, indicating a signed overflow. Otherwise, it is cleared. The "Z" or Zero flag is set if the sum (stored into the accumulator) is zero, otherwise, it is cleared. The "C" or carry is set if the sum of the unsigned addends exceeds 255 (binary mode) or 99 (decimal mode).

Flags

N	V	E	B	D	I	Z	C
N	V	-	-	-	-	Z	C

And memory logically with accumulator AND

A=A.and.M

Addressing Mode	Abbrev.	Opcode
immediate	IMM	29
base page	BP	25
base page indexed X	BP,X	35
absolute	ABS	2D
absolute indexed X	ABS,X	3D
absolute indexed Y	ABS,Y	39
base page indexed indirect X	(BP,X)	21
base page indirect indexed Y	(BP),Y	31
base page indirect indexed Z	(BP),Z	32

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

The AND instructions perform a logical "and" between data bits fetched from memory and the accumulator bits. The results are then stored in the accumulator. For each accumulator and corresponding memory bit that are both logical 1's, the result is a 1. Otherwise it is 0.

The "N" or Negative flag will be set if the bit 7 result is a 1. Otherwise it is cleared. The "Z" or Zero flag is set if all result bits are zero, otherwise, it is cleared.

Flags	N V E B D I Z C
	N - - - - - - Z -

Arithmetic shifts, memory or accumulator, left or right ASL ASR ASW

ASL	Arithmetic shift left A or M	A<1 or M<1
ASR	Arithmetic shift right A or M	A>1 or M1
ASW	Arithmetic shift left M (word)	Mw<1

		Opcodes		
Addressing Mode	Abbrev.	ASL	ASR	ASW
register (A)		0A	43	
base page	BP	06	44	
base page indexed X	BP,X	16	54	
absolute	ABS	0E		CB
absolute indexed X	ABS,X	1E		

Bytes	Cycles	Mode
1	1	register (ASL)
1	2	register (ASR)
2	4	base page (byte) non-indexed, or indexed X
3	5	absolute non-indexed, or indexed X
3	7	absolute (ASW)

The ASL instructions shift a single byte of data in memory or the accumulator left (towards the most significant bit) one bit position. A 0 is shifted into bit 0.

The "N" or Negative bit will be set if the result bit 7 is (operand bit 6 was) a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 7 was) a 1. Otherwise, it is cleared.

The ASR instructions shift a single byte of data in the accumulator right (towards the least significant bit) one bit position. Since this is an arithmetic shift, the sign of the operand will be maintained. The "N" or Negative bit will be set if bit 7 (operand and result)is a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 0 was) a 1. Otherwise, it is cleared.

The ASW instruction shifts a word (two bytes) of data in memory left (towards the most significant bit) one bit position. A zero is shifted into bit 0. The "N" or Negative bit will be set if the result bit 15 is (operand bit 14 was) a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits (both bytes) are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 15 was) a 1. Otherwise, it is cleared.

Flags	N	V	E	B	D	I	Z	C
	N	-	-	-	-	-	Z	C

Bit Test (A.and.M) BIT

Addressing Mode	Abbrev.	Opcode
immediate	IMM	89
base page	BP	24
base page indexed X	BP,X	34
absolute	ABS	2C
absolute indexed X	ABS,X	3C

Bytes	Cycles	Mode
2	2	Immediate
2	4	base page non-indexed, or indexed X
3	5	absolute non-indexed, or indexed X

The BIT testing instructions perform a logical "and" between data fetched from memory, and the accumulator. The result is not stored.

The "N" flag will be set if bit 7 of the memory operand is a 1. Otherwise it is cleared. The "V" flag will be set if bit 6 of the memory operand is a 1. Otherwise, it is cleared. The "Z" or Zero flag will be set if all result bits of the "and" operation are zero. Otherwise, it is cleared.

Flags	N	V	E	B	D	I	Z	C
	7	6	-	-	-	-	Z	-

Branch if memory bit reset or set BBR , BBS

Opcode to test bit

	0	1	2	3	4	5	6	7	
BBR	0F	1F	2F	3F	4F	5F	6F	7F	Branch if bit reset
BBS	8F	9F	AF	BF	CF	DF	EF	FF	Branch if bit set

Bytes	Cycles	Mode
3	4	base-page (test), byte-relative (branch)

The BBR instructions test a single bit within a Base-Page memory location. If the bit is reset (or 0) the byte-offset relative branch is taken.

Similarly, the BBS performs a the same test. If the bit is set (or 1) the branch is taken.

Use of these opcodes are discouraged, as they may be unavailable in future products.

The relative offset of the branch is referenced to the BBR or BBS opcode+3, or the location after the three BBR or BBS instruction bytes.

Flags N V E B D I Z C
- - - - - - - -

Branch conditional or unconditional BCC BCS BEQ BMI BNE BPL BRU BVC BVS

Opcode Title	Opcode Byte Relative	Opcode Word Relative	Opcode Purpose
BCC	90	93	Branch if Carry Clear
BCS	B0	B3	Branch if Carry Set
BEQ	F0	F3	Branch if EQual (Z flag set)
BMI	30	33	Branch if MInus (N flag set)
BNE	D0	D3	Branch if Not Equal (Z flag clear)
BPL	10	13	Branch if PLus (N flag clear)
BRU	80	83	BRanch Unconditional
BVC	50	53	Branch if oVerflow Clear
BVS	70	73	Branch if oVerflow Set

Bytes	Cycles	Mode
2	2	byte-relative
3	3	word-relative

All branches of this type are taken, if the condition indicated by the opcode is true. All branch relative offsets are referenced to the branch opcode location+2. This means that for byte-relative, the offset is relative to the location after the two instruction bytes. For word-relative, the offset is relative to the last of the three instruction bytes.

Flags N V E B D I Z C
- - - - - - - -

Break (force an interrupt) BRK

Bytes	Cycles	Mode	Opcode
2	7	implied	00 (stack)< PC +1wP, SP <SP-3

The BRK instruction causes the processor to enter the IRQ or Interrupt ReQuest state. The program counter (now incremented by 2), bytes PCH and PCL, and the processor status register P, are pushed onto the stack. (This causes the stack pointer SP to be decremented by 3.) Then the program counter bytes PCL and PCH are loaded from memory addresses FFFE and FFFF, respectively.

The BRK differs from an externally generated interrupt request (IRQ) as follows. The program counter value stored on the stack is PC+2, or the address of the BRK opcode+2. On return from interrupt, the processor will return to the BRK address+2, thus skipping the opcode byte, and a following "dummy" byte. A normal IRQ will not add 2, so that a return will execute the interrupted opcode. Also, when the P register is pushed onto the stack, the B or "break" flag is set, to indicate that the interrupt was software generated. All outside interrupts push P with the B flag cleared.

Flags N V E B D I Z C
- - - - - - - -

Branch to subroutine BSR

Bytes	Cycles	Mode	Opcode	
3	5	word-relative	63	(stack) < PC +2W, SP < SP-2

The BSR Branch to SubRoutine instruction pushes the two program counter bytes PCH and PCL onto the stack. It then adds the word-relative signed offset to the program counter. The relative offset is referenced to the address of the BSR opcode+2, hence, it is relative to the third byte of the three-byte BSR instruction. The return address, on the stack, also points to this address. This was done to make it compatible with the RTS functionality, and to be consistant will other word-relative operations.

Flags N V E B D I Z C
- - - - - - - -

Clear processor status bits

CLC CLD CLE CLI CLV

	Opcode	Cycles	Flags N V E B D I Z C
CLC Clear the Carry bit	18	1	- - - - - - - 0
CLD Clear the Decimal mode bit	D8	1	- - - - 0 - - -
CLE Clear stack Extend disable bit	02	2	- - 0 - - - - -
CLI Clear Interrupt disable bit	58	2	- - - - - 0 - -
CLV Clear the Oveflow bit	B8	1	- 0 - - - - - -

Bytes	Mode
1	implied

All of the P register bit clear intructions are a single byte long. Most of them require a single CPU cycle. The CLI and CLE require 2 cycles. The purpose of extending the CLI to 2 cycles, is to enable an interrupt to occur immediately, if one is pending. Interrupts cannot occur after single cycle instructions.

Compare registers with memory CMP CPX CPY CPZ CMP

Compare accumulator with memory (A-M)
CPX Compare index X with memory (X-M)
CPY Compare index Y with memory (Y-M)
CPZ Compare index Z with memory (Z-M)

Opcodes

Addressing Mode	Abbrev.	CMP	CPX	CPY	CPZ
immediate	IMM	C9	E0	C0	C2
base page	BP	C5	E4	C4	D4
base page indexed X	BP,X	D5			
absolute	ABS	CD	EC	CC	DC
absolute indexed X	ABS,X	DD			
absolute indexed Y	ABS,Y	D9			
base page indexed indirect X	(BP,X)	C1			
base page indirect indexed Y	(BP),Y	D1			
base page indirect indexed Z	(BP),Z	D2			

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y

3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

Compares are performed by subtracting a value in memory from the register being tested. The results are not stored in any register, except the following status flags are updated.

The "N" or Negative flag will be set if the result is negative (assuming signed operands), otherwise it is cleared. The "Z" or Zero flag is set if the result is zero, otherwise it is cleared. The "C" or carry flag is set if the unsigned register value is greater than or equal to the unsigned memory value.

Flags N V E B D I Z C
N - - - - - Z C

Decrement Registers or Memory DEC DEW DEX DEY DEZ

DEC	Decrement accumulator or memory	A-1 or M -1
DEW	Decrement a memory word	Mw-1
DEX	Decrement index X	X -1
DEY	Decrement index Y	Y-1
DEZ	Decrement index Z	Z-1

		Opcodes				
Addressing Mode	Abbrev.	DEC	DEW	DEX	DEY	DEZ
implied	3A	CA	88	3B		
base page	BP	C6	C3			
base page indexed X	BP,X	D6				
absolute	ABS	CE				
absolute indexed X	ABS,X	DE				

Bytes	Cycles	Mode
1	1	register
2	4	base page (byte) non-indexed, or indexed X
2	6	base page (word)
3	5	absolute non-indexed, or indexed X

The DEC (accumulator), DEX, DEY, and DEZ instructions are single-byte, single-cycle, and decrement (or subtract 1 from) the specified register.

The DEC (memory), and DEW (memory) instructions decrement a byte or word, respectively, in memory. The "N" or "negative" flag is set if the result value is negative. Otherwise, it is cleared. The "Z" or "zero" flag is set if the result of the decrement is zero. Otherwise, it is cleared.

Flags N V E B D I Z C
N - - - - - Z -

Exclusive OR accumulator logically with memory EOR
A=A.or.M.and..not.(A.and.M)

Addressing Mode	Abbrev.	Opcode
immediate	IMM	49
base page	BP	45
base page indexed X	BP,X	55
absolute	ABS	4D
absolute indexed X	ABS,X	5D
absolute indexed Y	ABS,Y	59

base page indexed indirect X	(BP,X)	41
base page indirect indexed Y	(BP),Y	51
base page indirect indexed Z	(BP),Z	52

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

The EOR instructions perform an "exclusive or" between bits fetched from memory and the accumulator bits. The results are then stored in the accumulator. For each accumulator or corresponding memory bit that are different (one 1, and one 0) the result is a 1. Otherwise it is 0.

The "N" or Negative flag will be set if the bit 7 result is a 1. Otherwise it is cleared. The "Z" or Zero flag is set if all result bits are zero, otherwise, it is cleared.

Flags	N V E B D I Z C
	N - - - - - Z -

Increment Registers or Memory INC INW INX INY INZ

INC	Increment accumulator or memory	A+1 or M+ 1
INW	Increment a memory word	Mw+1
INX	Increment index X	X+1
INY	Increment index Y	Y+1
INZ	Increment index Z	Z+1

			Opcodes			
Addressing Mode	Abbrev. INC		INW	INX	INY	INZ
implied	1A	E8	C8	1B		
base page	BP		E6	E3		
base page indexed X	BP,X		F6			
absolute	ABS		EE			
absolute indexed X	ABS,X		FE			

Bytes	Cycles	Mode
1	1	register
2	4	base page (byte) non-indexed, or indexed X
2	6	base page (word)
3	5	absolute non-indexed, or indexed X

The INC (accumulator), INX, INY, and INZ instructions are single-byte, single-cycle, and increment (or add 1 to) the specified register. The INC (memory), and INW (memory) instructions increment a byte or word, respectively, in memory. The "N" or "negative" flag is set if the result value is negative. Otherwise, it is cleared. The "Z" or "zero" flag is set if the result of the increment is zero. Otherwise, it is cleared.

Flags	N V E B D I Z C
	N - - - - - Z -

Jump to new location JMP

Addressing Mode	Abbrev .	Opcode	bytes	cycles
absolute	ABS	4C	3	3
absolute indirect	(ABS)	6C	3	5
absolute indexed indirect X	(ABS,X)	7C	3	5

The JMP instructions cause the word value read from memory to be loaded into the Program Counter, PC

Flags N V E B D I Z C
- - - - - - - -

Jump to subroutine JSR

Addressing Mode	Abbrev.	Opcode	bytes	cycles
absolute	ABS	20	3	5
absolute indirect	(ABS)	22	3	7
absolute indexed indirect X	(ABS,X)	23	3	7

The JSR Jump to SubRoutine instruction pushes the two program counter bytes PCH and PCL onto the stack. It then loads the program counter with the new address. The return address, stored on the stack, is actually the address of the JSR opcode+2, or is pointing to the third byte of the three-byte JSR instruction

Flags N V E B D I Z C
- - - - - - - -

Load registers LDA LDX LDY LDZ

LDA	Load Accumulator from memory	A
LDX	Load index X from memory	X
LDY	Load index Y from memory	Y
LDZ	Load index Z from memory	Z

Addressing Mode	Abbrev.	LDA	LDX	LDY	LDZ
immediate	IMM	A9	A2	A0	A3
base page	BP	A5	A6	A4	
base page indexed X	BP,X	B5		B4	
base page indexed Y	BP,Y		B6		
absolute	ABS	AD	AE	AC	AB
absolute indexed X	ABS,X	BD		BC	BB
absolute indexed Y	ABS,Y	B9	BE		
base page indexed indirect X	(BP,X)	A1			
base page indirect indexed Y	(BP),Y	B1			
base page indirect indexed Z	(BP),Z	B2			
stack vector indir indexed Y	(d,SP),Y	E2			

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z
2	6	stack vector indirect indexed Y

These instructions load the specified register from memory. The "N" or Negative flag will be set if the bit 7 loaded is a 1. Otherwise it is cleared. The "Z" or Zero flag is set if all bits loaded are zero, otherwise, it is cleared

Flags N V E B D I Z C
7 - - - - - Z -

Logical shift, memory or accumulator, right LSR
A>1 or M<M>1

Addressing Mode	Abbrev.	Opcodes LSR
register (A)		4A
base page	BP	46
base page indexed X	BP,X	56
absolute	ABS	4E
absolute indexed X	ABS,X	5E

Bytes	Cycles	Mode
1	1	register
2	4	base page non-indexed, or indexed X
3	5	absolute non-indexed, or indexed X

The LSR instructions shift a single byte of data in memory or the accumulator right (towards the least significant bit) one bit position. A 0 is shifted into bit 7 (the sign bit).

The "N" or Negative bit will be cleared. The "Z" or Zero flag is set if ALL result bits are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 0 was) a 1. Otherwise, it is cleared.

Flags N V E B D I Z C
R - - - - - Z C

ADD MAP OPCODE HERE

Negate (twos complement) accumulator NEG
A=-A

Addressing Mode	Opcode	Bytes	Cycles
implied	42	1	2

The NEG or "negate" instruction performs a two's-complement inversion of the data in the accumulator. For example, 1 becomes -1, -5 becomes 5, etc. The same can be achieved by subtracting A from zero.

The "N" or Negative flag will be set if the accumulator bit 7 becomes a 1. Otherwise it is cleared. The "Z" or Zero flag is set if the accumulator is (and was) zero.

Flags N V E B D I Z C
N - - - - - Z -

No-operation NOP

Addressing Mode	Opcode	Bytes	Cycles
implied	EA	1	1

Flags N V E B D I Z C
- - - - - - - -

The NOP instruction has no effect, except after a MAP in which case it is used to re-enable interrupts inhibited by the MAP opcode.

Or memory logically with accumulator ORA

A=A.or.M

Addressing Mode	Abbrev.	Opcode
immediate	IMM	09
base page	BP	05
base page indexed X	BP,X	15
absolute	ABS	0D
absolute indexed X	ABS,X	1D
absolute indexed Y	ABS,Y	19
base page indexed indirect X	(BP,X)	01
base page indirect indexed Y	(BP),Y	11
base page indirect indexed Z	(BP),Z	12

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

The ORA instructions perform a logical "or" between data bits fetched from memory and the accumulator bits. The results are then stored in the accumulator. For either accumulator or corresponding memory bit that is a logical 1, the result is a 1. Otherwise it is 0.

The "N" or Negative flag will be set if the bit 7 result is a 1. Otherwise it is cleared. The "Z" or Zero flag is set if all result bits are zero, otherwise, it is cleared.

Flags N V E B D I Z C

N - - - - - Z -

Pull register data from stack PLA PLP PLX PLY PLZ

		Opcode
PLA	Pull Accumulator from stack	68
PLX	Pull index X from stack	FA
PLY	Pull index Y from stack	7A
PLZ	Pull index Z from stack	FB
PLP	Pull Processor status from stack	28

Bytes	Cycles	Mode
1	3	register

The Pull register operations, first, increment the stack pointer SP, and then, load the specified register with data from the stack.

Except in the case of PLP, the "N" or Negative flag will be set if the bit 7 loaded is a 1. Otherwise it is cleared. The "Z" or Zero flag is set if all bits loaded are zero, otherwise, it is cleared.

In the case of PLP, all processor flags (P register bits) will be loaded from the stack, except the "B" or "break" flag, which is always a 1, and the "E" or "stack pointer Extend disable" flag, which can only be set by SEE, or cleared by CLE instructions.

```
Flags   N V E B D I Z C
        N - - - - - Z -  (except PLP)
        7 6 - - 3 2 1 0  (PLP only)
```

Push registers or data onto stack PHA PHP PHW PHX PHY PHZ

PHA Push Accumulator onto stack
PHP Push Processor status onto stack
PHW Push a word from memory onto stack
PHX Push index X onto stack
PHY Push index Y onto stack
PHZ Push index Z onto stack

		Opcodes					
Addressing Mode	Abbrev	PHA	PHP	PHW	PHX	PHY	PHZ
register		48	08		DA	5A	DB
word immediate	IMMw			F4			
word absolute	ABSw			FC			

Bytes	Cycles	Mode
1	3	register
3	5	word immediate
3	7	word absolute

These instructions push either the contents of a register onto the stack, or push two bytes of data from memory (PHW) onto the stack. If a register is pushed, the stack pointer will decrement a single address. If a word from memory is pushed, the stack pointer will decrement by 2. No flags are changed.

```
Flags   N V E B D I Z C
        - - - - - - - -
```

NOTE: word pushes are performed low-byte first. This means that the lower order byte pushed will become the high order byte on the stack.

Reset memory bits RMB
M=M.and.-bit
Opcode to reset bit

0	1	2	3	4	5	6	7
07	17	27	37	47	57	67	77

Bytes	Cycles	Mode
2	4	base-page

These instructions reset a single bit in base-page memory, as specified by the opcode. No flags are modified.
Flags N V E B D I Z C
- - - - - - - -

Use of these opcodes is discouraged , as they may be unavailable on a later product.

Rotate memory or accumulator, left or right ROL ROR ROW

ROL Rotate memory or accumulator left throught carry
ROR Rotate memory or accumulator right throught carry
ROW Rotate memory (word) left throught carry

		Opcodes		
Addressing Mode	Abbrev.	ROL	ROR	ROW
register (A)		2A	6A	
base page	BP	26	66	
base page indexed X	BP,X	36	76	
absolute	ABS	2E	6E	EB
absolute indexed X	ABS,X	3E	7E	

Bytes	Cycles	Mode
1	1	register
2	4	base page (byte) non-indexed, or indexed X
3	5	absolute non-indexed, or indexed X
2	6	absolute (word)

The ROL instructions shift a single byte of data in memory or the accumulator left (towards the most significant bit) one bit position. The state of the "C" or "carry" flag is shifted into bit 0.

The "N" or Negative bit will be set if the result bit 7 is (operand bit 6 was) a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 7 was) a 1. Otherwise, it is cleared

The ROR instructions shift a single byte of data in memory or the accumulator right (towards the least significant bit) one bit position. The state of the "C" or "carry" flag is shifted into bit 7.

The "N" or Negative bit will be set if bit 7 is (carry was) a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 0 was) a 1. Otherwise, it is cleared.

The ROW instruction shifts a word (two bytes) of data in memory left (towards the most significant bit) one bit position. The state of the "C" or "carry" flag is shifted into bit 0.

The "N" or Negative bit will be set if the result bit 15 is (operand bit 14 was) a 1. Otherwise, it is cleared. The "Z" or Zero flag is set if ALL result bits (both bytes) are zero. The "C" or Carry flag is set if the bit shifted out is (operand bit 15 was) a 1. Otherwise, it is cleared.

Flags N V E B D I Z C
N - - - - - Z C

Return from BRK, interrupt, kernal, or subroutine RTI RTN RTS

Operation	description	Opcode	bytes	cycles	
RTI	Return from interrupt	40	1	5	P,PCw(SP),SP 3
RTN #n	Return from kernal	62	2	7	PCw(SP)+1,SP 2+N
RTS	Return from subroutine	60	1	4	PCw(SP)+1,SP 2

The RTI or ReTurn from Interrupt instruction pulls P register data and a return address into program counter bytes PCL and PCH from the stack. The stack pointer SP is resultantly incremented by 3. Execution continues at the address recovered from the stack.

The RTS or ReTurn from Subroutine instruction pulls a return address into program counter bytes PCL and PCH from the stack. The stack pointer SP is resultantly incremented by 2. Execution continues at the address recovered + 1, since BSR and JSR instructions set the return address one byte short of the desired return address.

The RTN or ReTurn from kerNal subroutine is similar to RTS, except that it contains an immediate parameter N indicating how many extra bytes to discard from the stack. This is useful for returning from subroutines which have arguments passed to them on the stack. The stack pointer SP is incremented by 2 +N, instead of by 2, as in RTS.

Flags N V E B D I Z C
- - - - - - - - (RTN and RTS)
7 6 - - 3 2 1 0 (RTI)

Subtract memory from accumulator with borrow SBC
A=A-M+C-1

Addressing Mode	Abbrev.	Opcode
immediate	IMM	E9
base page	BP	E5
base page indexed X	BP,X	F5
absolute	ABS	ED
absolute indexed X	ABS,X	FD
absolute indexed Y	ABS,Y	F9
base page indexed indirect X	(BP,X)	E1
base page indirect indexed Y	(BP),Y	F1
base page indirect indexed Z	(BP),Z	F2

Bytes	Cycles	Mode
2	2	immediate
2	3	base page non-indexed, or indexed X or Y
3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z

The SBC instructions subtract data fetched from memory from the contents of the accumulator, assuming the "C" or "carry" flag was set. If "C" was clear, an additional count is subtracted. The results of the subtract is stored in the accumulator. If the "D" or Decimal Mode flag, in the processor status register, then a Binary Coded Decimal (BCD) subtract is performed.

The "N" or Negative flag will be set if the difference is negative, otherwise it is cleared. The "V" or Overflow flag will be set if the sign of the difference is different from the sign of both operands, indicating a signed overflow. Otherwise, it is cleared. The "Z" or Zero flag is set if the difference (stored into the accumulator) is zero, otherwise, it is cleared. The "C" or carry is set if the unsigned minuend (in the accumulator) is greater-than or equal-to the unsigned subtrahend (in memory). Otherwise, it is cleared.

Flags N V E B D I Z C
N V - - - - Z C

Set processor status bits

SEC SED SEE SEI

		Opcode	Cycles	Flags N V E B D I Z C
SEC	Set the Carry bit	38	1	- - - - - - - 1
SED	Set the Decimal mode bit	F8	1	- - - - 1 - - -
SEE	Set stack Extend disable bit	03	2	- - 1 - - - - -
SEI	Set Interrupt disable bit	78	2	- - - - - - S - -

Bytes	Mode
1	implied

All of the P register bit set intructions are a single byte long. Most of them require a single CPU cycle. The SEE and SEI require 2 cycles.

Set memory bits

SMB

M=M.or.bit

Opcode to set bit

0	1	2	3	4	5	6	7
87	97	A7	B7	C7	D7	E7	F7

Bytes	Cycles	Mode
2	4	base-page

These instructions set a single bit in base-page memory, as specified by the opcode. No flags are modified.
Use of this opcode is discouraged , as it may be unavailable on a later product.

Flags	N	V	E	B	D	I	Z	C
-	-	-	-	-	-	-	-	

Store registers

STA STX STY STZ

STA	Store Accumulator to memory	MA
STX	Store index X to memory	M X
STY	Store index Y to memory	MY
STZ	Store index Z to memory	MZ

Addressing Mode	Abbrev.	Opcodes STA	STX	STY	STZ
base page	BP	85	86	84	64
base page indexed X	BP,X	95		94	74
base page indexed Y	BP,Y		96		
absolute	ABS	8D	8E	8C	9C
absolute indexed X	ABS,X	9D		8B	9E
absolute indexed Y	ABS,Y	99	9B		
base page indexed indirect X	(BP,X)	81			
base page indirect indexed Y	(BP),Y	91			
base page indirect indexed Z	(BP),Z	92			
stack vector indirect indexed Y	(d,SP),Y	82			

Bytes	Cycle	Mode
2	3	base page non-indexed, or indexed X or Y

3	4	absolute non-indexed, or indexed X or Y
2	5	base page indexed indirect X, or indirect indexed Y or Z
2	6	stack vector indirect indexed Y

These instructions store the specified register to memory. No flags are affected.

Flags	N	V	E	B	D	I	Z	C
	-	-	-	-	-	-	-	-

Transfers (between registers) TAB TAX TAY TAZ TBA TSX TSY TXA TXS TYA TYS TZA

Symbol	Code	Flags N V E B D I Z C	Transfer from	to
TAB	5B	- - - - - - - -	accumulator	base page reg
TAX	AA	N - - - - - Z -	accumulator	index X reg
TAY	A8	N - - - - - Z -	accumulator	index Y reg
TAZ	4B	N - - - - - Z -	accumulator	index Z reg
TBA	7B	N - - - - - Z -	base page reg	accumulator
TSX	BA	N - - - - - Z -	stack ptr low	index X reg
TSY	0B	N - - - - - Z -	stack ptr high	index Y reg
TXA	8A	N - - - - - Z -	index X reg	accumulator
TXS	9A	- - - - - - - -	index X reg	stack ptr low
TYA	98	N - - - - - Z -	index Y reg	accumulator
TYS	2B	- - - - - - - -	index Y reg	stack ptr high
TZA	6B	N - - - - - Z -	index Z reg	accumulator

These instructions transfer the contents of the specified source register to the specified destination register. Any transfer to A, X, Y, or Z will affect the flags as follows. The "N" or "negative" flag will be set if the value moved is negative (bit 7 set), otherwise, it is cleared. The "Z" or "zero" flag will be set if the value moved is zero (all bits 0), otherwise, it is cleared. Any transfer to SPL or SPH will not alter any flags.

Bytes	Cycles	Mode
1	1	register

Test and reset or set memory bits TRB TSB

TRB Test and reset memory bits with accumulator (M.and.A),M.and.-A
TSB Test and set memory bits with accumulator (M.and.A),M.or.A

Addressing Mode	Abbrev.	Opcodes TRB	TS
base page	BP	14	04
absolute	ABS	1C	0C

These instructions test and set or reset bits in memory, using the accumulator for both a test mask, and a set or reset mask. First, a logical AND is performed between memory and the accumulator. The "Z" or "zero" flag is set if all bits of the result of the AND are zero. Otherwise it is reset.

The TSB then performs a logical OR between the bits of the accumulator and the bits in memory, storing the result back into memory.

The TRB, instead, performs a logical AND between the inverted bits of the accumulator and the bits in memory, storing the result back into memory.

Flags	N	V	E	B	D	I	Z	C
	-	-	-	-	-	-	Z	-

MAO Opcode MAP

Addressing Mode	Abbv	Opcode	Bytes	Cycles
Implied	MAP	5C	1	4

The C4510 memory coremapper allows the microprocessor to access up to 1 megabyte of memory. Here's how. The 6503 microprocessor can only access 64K bytes of memory because it only uses addresses of 16 bits. But the 4510 memory mapper allows these addresses to be redirected to new physical addresses to access different parts of a much larger memory, within the 64K byte confinement window.

The 64K window has been divided into eight blocks, and two regions, with four blocks in each region. Blocks 0 through 3 are in the "lower" region, and blocks 4 through 7 are in the "upper" region, as shown...

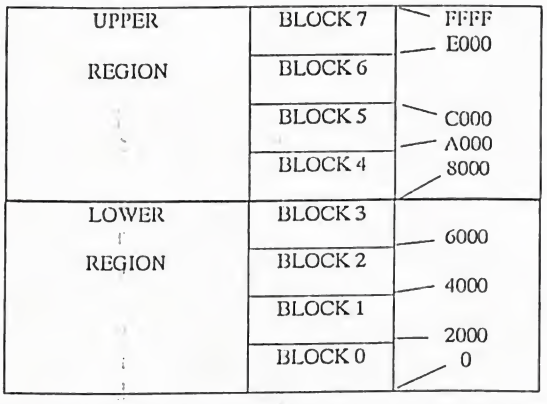

FIGURE 3 - MEMORY MAPPER 64K CONFINEMENT WINDOW

Each block can be programmed to be "mapped", or "non-mapped" via bits in the mapper's "mask" registers. Non-mapped means, simply, address out equals address in. Therefore, there are still only 64K bytes of non- mapped memory. Mapped, means that address out equals address in plus some offset. The offset is programmed via the mapper's "offset" registers. There are two "offset" registers. One is for the lower region, and one is for the upper region.

The low-order 8 address bits are never mapped. The offsets are only added to the 12 high-order address bits. This means the smallest unit you can map to is 256 bytes or one page.

The 4510 has an output (MAP/) which lets the outside world know when the processor is accessing a mapped (MAP/ is low) or non-mapped (MAP/ is high) address. This is useful for systems where you may want I/O devices to be at fixed (non-mapped) addresses, and only memory at mapped addresses.

It is possible, and likely, to have mapped, and unmapped memory at the same physical address. And, with offset registers set to zero, mapped addresses will match unmapped ones. The only difference is the MAP/ signal to tell whether the address is mapped or unmapped. The MAp operation transfers the contents of the A,X,Y, and Z registers to the memory mapper registers A,X,Y, and Z. All subsequent interrupts are inhibited until a NOP is executed.

Flags NVEBDIZC
- - - - - - -

7	6	5	4	3	2	1	0	BIT
LOWER OFF 15	LOWER OFF 14	LOWER OFF 13	LOWER OFF 12	LOWER OFF11	LOWER OFF 10	LOWER OFF 9	LOWER OFF 8	A
MAP BLK 3	MAP BLK 2	MAP BLK 1	MAP BLK 0	LOWER OFF 19	LOWER OFF 18	LOWER OFF 17	LOWER OFF 16	X
UPPER OFF 15	UPPER OFF 14	UPPER OFF 13	UPPER OFF 12	UPPER OFF 11	UPPER OFF 10	UPPER OFF 9	UPPER OFF 8	Y
MAP BLK 7	MAP BLK 6	MAP BLK 5	MAP BLK 4	UPPER OFF 19	UPPER OFF 18	UPPER OFF 17	UPPER OFF 16	Z

After executing the MAP opcode, all interrupts are inhibited. This is done to allow the operating system to complete a mapping sequence without fear of getting an interrupt. An interrupt occuring before the proper stack-pointer is set will cause return address data to be written to an undesired area.

Upon completing the mapping sequence, the operating system must remove the interrupt inhibit by executing an NOP opcode. Note that application software may execute NOPs with no effect.

To program the mapper, the operating system must load the A, X, Y, and Z registers with the following information, and execute a MAP opcode.

2.5 PERIPHERAL CONTROL FUNCTIONS

2.5.1 I/O PORTS

Ports A, B and D each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). Port E consists of a 2-bit PR and DDR registers. If a bit in the DDR is set to one, the corresponding bit in the PR is an output, if a DDR bit is set to a zero, the corresponding PR bit is defined as an input. On a READ, the PR bit reflects the information present on the actual port pins (PRA0-PRA7, PRB0-PRB7, PRC2, PRD0-PRD7, PRE0-PRE1) for both input and output bits. All ports have passive pull-up devices as well as active pull-ups, providing both CMOS and TTL compatibility. In addition to normal I/O operation, PRB6, RB7, PRD6 and PRD7 also provide timer output functions (refer to Control Register section, 2.5.8).

Only bit PC2 and DPC2 of PORT C meet the above description. The other bits function as described in the following:

PC0, PC1
These signals are simply register bits. When read, they will reflect the value previously written to the PRC register.

PC4
This bit is a "high" if it's configured as input (DPC4 is a "low"). If configured as output (DPC4 is a "high"), the

bit will reflect its previous written value when PORT C is read. Then the PRC46 pin is pulled "low" if PC4 is "high"; otherwise, PRC46 is pulled-up through passive resistor.

PC5
This bit is a "high" if it's configured as input (DPC5 is a "low"). If configured as output (DPC5 is a "high"), the bit will reflect its previous written value when PORT C is read. Then the PRC57 pin is pulled "low" if PC5 is "high"; otherwise, PRC57 is pulled-up through passive resistor.

PC6,PC7
These bits are always configured as inputs. When PORT C (PRC) is read, PC6 and PC7 will reflect the values on the PRC46 and PRC57 pins, respectively.

2.5.2 HANDSHAKING

Handshaking on data transfers can be accomplished using the PC/ output pin and either the FLAGA/ or FLAGB/ input pin. The PC/ line will go low and stay low for two cycles, two cycles after a read or write to PORT D. This is required to meet Centronics Parallel Interface specs. The PC/ line can be used to indicate "data ready" at PORT D or "data accepted" from PORT D. Handshaking on 16-bit data transfers (using either PORT A or B and then PORT D) is possible by always reading or writing PORT A or PORT B first. The FLAG/ lines are negative edge sensitive inputs which can be used for receiving the PC/ output from other 4510 devices, or as general purpose interrupt inputs. A negative transition on FLAGA/ or FLAGB/ will set the FLAGA or FLAGB interrupt bits, respectively.

2.5.3 INTERVAL TIMERS
(Timer A, Timer B, Timer C, Timer D)

Each interval timer consists of a 16-bit read-only Timer Counter and a16-bit write-only Timer Latch (prescaler). Data written to the timer are latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked in pairs for extended operations (TIMER A may be linked with Timer B; TIMER C may be linked with TIMER D). The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT inputs, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions (see bits functional description in section 2.5.8 below):

Start/Stop
Each timer may be started or stopped by the microprocessor at any time by writing to the START/STOP bit of the corresponding control register (CRA, CRB, CRB or CRC).

PRB, PRD On/Off
Control bits allow any of the timer outputs to appear on a PORT B or PORT D output line (PRB6 for TIMER A, PRB7 for TIMER B, PRD6 for TIMER C and PRD7 for TIMER D). Note that this function overrides the DDRB control bit and forces the appropiate PB or PC line to be an output.

Toggle/Pulse
Control bits select the ouputs applied to PORT B and PORT D. On every timer underflow the ouput can either toggle or generate a single positive pulse of one cycle duration. The Toggle output is set high whenever the appropiate timer is started and is set low by RESET/.

One-Shot/Continuous
Control bits select either timer mode. In one-shot mode, the timer will count down from the latched value to zero,

generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously.

Force Load
A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

Input Mode
Control bits allow selection of the clock used to decrement the timer. TIMER A or TIMER C can count C1MHZ clock pulses or external pulses applied to the CNTA or CNTB, respectively. The C1MHZ clock is obtained after internally dividing the C7MHZ by a factor of seven.

TIMER B can count C1MHZ clock pulses, external pulses applied to the CNTA input, TIMER A underflow pulses or TIMER A underflow pulses while the CNTA pin is held high.

TIMER D can count C1MHZ clock pulses, external pulses applied to the CTNB input, TIMER C underflow pulses or TIMER C underflow pulses while the CNTB pin is held high. The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

2.5.4 Time of Day Clocks (TODA, TODB)

The TODA and TODB clocks are special purpose timers for real-time applications. Each clock, TODA or TODB, consists of a 24-hour (AM/PM) clock with 1/10th second resolution. Each is organized into four registers: 10ths of seconds (TODATS, TODBTS), Seconds (TODAS, TODBS), Minutes (TODAM, TODBM) and Hours (TODAH, TODBH). The AM/PM flag is in the MSB of the Hours register for easy testing. Each register reads out in BCD format to simplify conversion for driving displays, etc. Each TOD requires a 10HZ clock input to keep accurate timing. This 10HZ clock is generated by dividing the C7MHz clock input by a factor of 102273 for NTSC (60Hz) applications, or a factor of 101339 for PAL (50Hz) applications. The divider ratio is selected by the TODA IN and the TODB IN bits of the Control Registers, CRA and CRC, respectively (see 2.5.8).

In addition to time-keeping, a programmable ALARM is provided for generating an interrupt at the desired time, from either of the TOD clocks. The ALARM registers registers are located at the same addresses as the corresponding TODA and TODB registers. Access to the ALARM is governed by bit 7 in the Control Registers CRB and CRD. The ALARM registers are write-only; any read of a TOD address will read time regardless of the state of the ALARM access control bits.

A specific sequence of events must be followed for proper setting an reading of each TOD. A TOD is automatically stopped whenever a write to the corresponding Hours register occurs. The TOD will not start again until after a write to the proper 10ths of seconds register. This assures that a TOD will always start at the desired time. Since a carry from one stage to the next can occur at any time with respect to a read operation, a latching function is included to keep all Time of Day information constant during a read sequence. All four registers of each TOD latch on a read of the corresponding Hours register and remain latched until after a read of the corresponding 10ths of second register. A TOD continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly", provided that any read of the Hours register is followed by a read of the proper 10ths of seconds, to disable the latching.

2.5.5 Serial Ports (SDRA, SDRB)

Each serial port is a buffered, 8-bit synchronous shift register system. A control bit (CRA SPA bit, CRC SPB bit) selects input or output mode for either the SDRA or SDRB port.

In input mode, data on the SPA or SPB pin is shifted into the corresponding shift register on the rising edge of the signal applied to the CNTA or CNTB pin, respectively. After 8 CNTA pulses , the data in the shift register is dumped into the SERIALA Data Register (SDRA) and an interrupt is generated, SPA bit is set in register ICRA. After 8 CNTB pulses , the data in the shift register is dumped into the SERIALB Data Register (SDRB) and an interrupt is generated, SPB bit is set in register ICRB.

In the output mode, TIMER A is used for the baud rate generator of serial port A, Timer C for serial port B. Data is shifted on an SP pin at half the underflow rate of the TIMER used. The maximum baud rate possible is C1MHz divided by four, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to Serial Data Register (provided the proper TIMER used is running and in continuous mode). The clock signal derived from TIMER A would appear as an output on the CNTA pin; the one from TIMER C would appear otn the CNTB pin. The data in the Serial Data Register will be loaded into its corresponding shift register then shift out to the SPA or SPB pin when a CNTA or CNTB pulse occurs, respectively. Data shifted out becomes valid on the falling edge of its CNT clock and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will continue. If the microprocessor stays one byte ahead of the shift register, transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear on this format.

The bidirectional capability of each of the Serial Ports and CNT clocks allows many 4510 to be connected to a common serial communication bus on which one Serial Port would act as a master and source for data and shift clock, while the other Serial Port (and all other ports from other 4510 devices) would act as slaves. All the CNT and SP outputs are open drain to allow such a common bus. Protocol for master/slave selection can be transmitted over the serial bus, or via dedicated handshaking lines.

2.5.6 FAST SERIAL MODE

The FAST SERIAL logic consists of a 2-bit write-only register, which resides in location 0001 (hex). Upon reset, both bits in the register are forced low, which allows the device to operate as normal (the CNTA, SPA, PRC57 and FLAGA/ lines will not be affected).

Bit 7 of the FAST SERIAL register is the Fast Serial Mode disable bit (DMODE* bit).

Bit 6 of the FAST SERIAL register is the FSDIR* bit. When the DMODE* bit is set high, the FSDIR* bit will be used as an output to control the fast serial data direction buffer hardware, and as an input to sense a fast disk enable signal. This function will affect the CNTA, SPA, PRC57 and FLAGA/ lines as summarized in the following table.

DMODE*	FSDIR	FUNCTION
0	X	Fast Serial mode is disabled.
1	0	INPUT MODE. Both the CNTA and the SPA lines will behave as outputs. The CNTA output will reflect the state of the FLABA/ pin, whereas the SPA output will reflect the state of the PRC57 pin.
1	1	OUTPUT MODE. Both the FLAGA/ and PRC57 lines will behave as outputs. The FLAGA/ ouput will reflect the state

of the CNTA pin, whereas the PRC57 output will reflect that of the SPA pin.

2.5.7 Interrupt Control Registers (ICRA, ICRB)

These registers control the following sources of interrupts:

i. Underflows from TIMER A, TIMER B, TIMER C and TIMER D
ii. TODA ALARM and TODB ALARM.
iii. SERIALA and SERIALB Port full/empty conditions.
iv. FLAGA/ and FLAGB/ low transitions.

The ICRA and ICRB registers each provides masking and interrupt information. ICRA and ICRB each consists of a write-only MASK register and a read-only DATA register. Any interrupt will set the corresponding bit in the DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of its corresponding DATA register and bring the IRQ/ pin low. In a multi-chip system, the IR bit (IRA of ICRA or IRB of ICRB) can be polled to detect which chip has generated an interrupt request. The interrupt DATA register is cleared and the IRQ/ line returns high following a read of the DATA register. Since each interrupt sets and interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling either of the IR bits will cause its corresponding DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA registers if any polled interrupts were present.

Both MASK (ICRA, ICRB) registers provide convenient control of individual mask bits. When writing to a MASK register, if bit 7 of the data written (corresponding to AS/C in ICRA, or BS/C in ICRB) is a ZERO, any mask bit written with a one will be cleared, while those bits written with a zero will be unaffected. In order for an interrupt flag to set the IR bit and generate an Interrupt Request, the corresponding MASK bit must be set in the corresponding MASK Register.

2.5.8 Control Registers (CRA, CRB, CRC, CRD)

CRA (0XE):

BIT	Bit Name	Function
0	STARTA	1=START TIMER A, 0=STOP TIMER A. This bit is automatically reset when TIMER A underflow occurs during oneshot mode.
1	PRB6 ON	1=TIMER A output appears on PRB6, 0=PRB6 normal port operation.
2	OUT-A MODE	1=TOGGLE output applied on port PRB6 0=PULSE output applied on port PRB6.
3	RUN-A MODE	1=ONE-SHOT TIMER A operation, 0=CONTINUOUS TIMER A operation.
4	LOADA	1=FORCE LOAD on TIMER A (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect).
5	TMRA INMODE	1=TIMER A counts positive CNTA transitions, 0=TIMER A counts internal C1MHZ pulses.
6	SPA MODE	1=SERIAL A PORT output mode (CNTA sources shift clock), 0=SERIAL A PORT input mode (external shift clock on CNTA)

7	TODA IN	1=50 Hz operation. C7MHZ divided down by 101339 to generate TODA input of 10 Hz. 0=60 Hz operation. C7MHZ divided down by 102273 to generate TODA input of 10 Hz

CRB (0XF):

(Bits 0-4 of the CRB register operate identically to bits 0-4 of the CRA register, except that functions now apply to TIMER B and bit 1 controls the output of TIMER B on PRB7).

BIT	Bit Name	Function
5,6	TIMERB INMODE	Bits 5 and 6 select one of four input modes for TIMER B as follows:

CRB6	CRB5	
0	0	TIMER B counts C1MHz pulses.
0	1	TIMER B counts positive CNTA transitions.
1	0	TIMER B counts TIMERA underflow pulses.
1	1	TIMER B counts TIMERA underflows while CNTA is high.

7	ALARM TODA	1=writing to TODA registers sets ALARM, 0=writing to TODA registers sets TODA clock.

CRC (1XE):

BIT	Bit Name	Function
0	STARTC	1=START TIMER C, 0=STOP TIMER C. This bit is automatically reset when TIMER C underflow occurs during oneshot mode.
1	PRD6 ON	1=TIMER C output appears on PRD6 0=PRD6 normal port operation.
2	OUT-C MODE	1=TOGGLE output applied on port PRD6, 0=PULSE output applied on port PRD6.
3	RUN-C MODE	1=ONE-SHOT TIMER C operation, 0=CONTINUOUS TIMER C operation.
4	LOADC	1=FORCE LOAD on TIMER C (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect).
5	TMRC INMODE	1=TIMER C counts positive CNTB transitions, 0=TIMER C counts internal C1MHZ pulses.
6	SPB MODE	1=SERIAL B PORT output mode (CNTB sources shift clock), 0=SERIAL B PORT input mode (external shift clock on CNTB)

7	TODB IN	1=50 Hz operation. C7MHZ divided down by 101339 to gene rate TODB input of 10 Hz 0=60 Hz operation. C7MHZ divided down by 102273 to generate TODB input of 10 Hz

CRD (1XF):
(Bits 0-4 of the CRD register operate identically to bits 0-4 of the CRD register, except that functions now apply to TIMER D and bit 1 controls the output of TIMER D on PRD7).

BIT	Bit Name	Function
5,6	TIMERD	Bits 5 and 6 select one of four input modes for TIMER D INMODE as follows:

CRD6	CRD5	
0	0	TIMER D counts C1MHz pulses.
0	1	TIMER D counts positive CNTB transitions.
1	0	TIMER D counts TIMERC underflow pulses.
1	1	TIMER D counts TIMERC underflows while CNTB is high.

7	ALARM TODB	1=writing to TODB registers sets ALARM, 0=writing to TODB registers sets TODA clock.

2.6 UART OPERATION

The device contains seven registers to control the different UART modes of operation. Section 2.2 describes how to access these registers.

The UART modes can be programmed by accessing the UART control register, URCR, whose bits function as described below.

2.6.1 UART Control Register (URCR)

BIT	Bit Name	Function
0	PARITY EVEN	1=Even Parity. If parity is enabled, the transmitter will assert the parity bit (P) to a low when "even" parity data is transmitted, otherwise it will pull it high. The receiver checks that the parity bit is asserted, or low, if the data received has even parity; if the bit is not asserted, the device will indicate a parity error. 0=Odd Parity. If parity is enabled, the transmitter will pull the parity bit (P) low, when "odd" parity data is transmitted, otherwise it will pull it high. The receiver checks that the parity bit is asserted if the data received has odd parity; if the bit is not asserted when data had odd parity, the device will indicate a parity error.
1	PARITY EN	1= Parity Enabled. 0= Parity Disabled. The transmitter and receiver will not allocate a parity bit in the data, instead a stop bit will be used in its place. See the Data Configuration chart below.

2,3 CHAR LENGTH

These two bits are used to select the number of bits per character to be transmitted or received. 5,6,7 or 8 bits per character may be selected as follows:

(3) (2)

CH1	CH0	
0	0	eight bits per character
0	1	seven bits per character
1	0	six bits per character
1	1	five bits per character

4,5 UART MODE

These two bits select whether operations will be asynchronous or synchronous for the transmitter and/or receiver. The actual selection is done as follows:

(5) UM1	(4) UM0	
0	0	both transmitter and receiver operate in asynchronous mode
0	1	receiver operates in synchronous mode, transmitter in asynchronous mode.
1	x	receiver operates in asynchronous mode, transmitter in synchronous mode.

BIT	Bit Name	Function
6	RCVR EN	0= Receiver is disabled.

1= Receiver is Enabled. To provide noise immunity, the duration of a bit interval is segmented into 16 sub-intervals. This is also used to verify that a high to low transition (START bit) on the RXD line is valid (stays low) at the half point of a bit duration; if not valid, operation will not start. If after an idle period, a high to low transition is detected on the RXD line and is verified to be low, the receiver will have synchronized itself to the incoming character for the duration of the character. Received data is then sampled or latched in the center of a bit time to determine the value of the remaining bits. The LSB of the data is the leading bit received. Any unused high order register bits will be set "high". The receiver expects the data to have only one parity bit (when parity is enabled) and one stop bit. At the end of the character reception, the receiver will check whether any errors have occured and will update the status register (URSR) accordingly. In addition, if no errors were encountered the receiver will load the contents of the shift register into the Receiver Data Register, eliminating parity and stop bits.

In synchronous mode, the receiver will reconfigure its Data Register and Shift Register so that only 8 databits are always accepted on the RXD line. This mode only works if an external clock is applied on the PRC2 input line, which is used to shift the bits into the Receiver Shift Register. Data on the RXD is latched at the rising edge of the external clock applied in PRC2.

7 XMITR EN

0= Transmitter is disabled

1= Transmitter is Enabled. Transmitter will start operation once the microprocessor writes data to the transmitter data register (DREG), after which the Transmitter Shift Register is loaded and the start bit is placed on the TXD line. The LSB of the data is the leading bit being transmitted. The Transmitter is "doubled buffered" which means that the CPU can load a new character as soon as the previous one starts transmission This is indicated by the status register, bit 6 (URSR6- TEMPTY Data Register), which when set, it indicates that the data register is ready to accept the next character.The character data format is illustrated by figure 1.3.

In synchronous mode, the transmitter will reconfigure its Data Register and Shift Register so that only 8 data bits are always transmitted on the TXD line, eliminating all parity and stop bits. The external clock output will be placed in the PRC2 line and will shift the data out of the transmitter shift register. Data on the TXDline will change on the falling edge of the PRC2 signal, the external clock.

2.6.2 UART Status Register (URCR)

BIT	Bit Name	Function
0	RFULL	Receiver Data Register Full bit. This bit is forced to a low upon reset, or after the data register (DREG) is read. This bit is enabled only if the RCVER EN bit is set in the URCR register. The FULL bit is set when the character being received is transferred from the receiver shift register into the receiver data register. If an error is encountered in the character data, this bit will not be set and the proper error bit will be set in the URSR register.
1	OVR	Receiver Over-Run Error bit. This bit is cleared upon reset or after reading the receiver data register. This bit is set if the new received charater is attempted to be transferred from the receiver shift register before reading the last character from the data register. Therefore, the last character is preserved in the data register while the new received character is lost.
2	PRTY	Receiver Parity Error bit. This bit is cleared upon reset or after reading the receiver data register. The PRTY bit will be set when a parity error is detected on the received character, provided the PARITY EN bit is set and receiver is running asynchronously.
3	FRME	Receiver Frame Error bit. This bit is cleared upon reset or after reading the receiver data register. The FRME bit is set whenever the received character contains a low in the first stop-bit slot.
4	IDLE	Receiver Idle bit. When this bit is written to a "high", the status register bits 0-3 are disabled until the receiver detects 10 consecutive marks, highs, on the RXD line, at which time the IDLE bit is cleared. This bit is also cleared upon reset. This bit allows the microprocessor, or any external microprocessor device, to ignore the transmission of a character until the start of the next character.
5	ENDT	Transmitter End of Transmission bit. This bit is cleared upon reset or whenever data is written into the transmitter data register, DREG. Setting this bit would disable the Transmitter Empty bit, TEMPTY, until device completes transmission.
6	TEMPTY	Transmitter data register empty bit. Upon reset (RESET/ is low) TEMPTY is set to high. this bit is cleared when the processor writes new data into the transmitter data register, DREG. The bit is set after all the bits in DREG are transferred into the transmitter shift register
7	TDONE	This bit is cleared when the RESET/ line is asserted or when the DREG dumps its contents into the shift register. When this bit is set, it indicates that the

2.6.3 UART Interrupt Registers (URIEN and URIFG)

BIT	Bit Name	Function
7	XMTR-IRQEN	When the XMTR-IRQEN bit is set , both the IRQ/ output line and the XMTFLG bit are asserted whenever either one of the following two conditions are met: 1. TEMPTY is set and ENDT is cleared. or, 2. Both TEMPTY and TDONE are set..
6	RCVR-IRQEN	When the RCVR-IRQEN bit is set, both the IRQ/ output line and the RCVFLG bit are asserted whenever either RFULL, OVR, PRTY, or FRME is set in the status register.
5	XMTR-NMIEN	When the XMTR-NMIEN bit is set, both the IRQ/ output line and the XMTFLG bit s are asserted whenever either one of the following conditions are met: 1. TEMPTY is set and ENDT is cleared. or, 2. Both TEMPTY and TDONE are set.
4	RCVR-NMIEN	When the RCVR-NMIEN bit is set, both the IRQ/ output line and the RCVFLG bit are asserted whenever either RFULL, OVR, PRTY or FRME are set in the status register.

2.6.4 BAUD RATE GENERATION

Any BAUD RATE canbe generated by using the following formula:

$$\text{Baud Rate} = \frac{\text{URCLK}}{16(\text{COUNT}+1)} \quad \text{or,} \qquad \text{COUNT} = \frac{\text{URCLK}}{16 \times \text{BaudRate}} - 1$$

Where URCLK = C7MHz input --7.15909 Mhz NTSC, &.09375 MHz PAL
COUNT = value loaded in BAUD RATE latches

The following table shows some of the most common data rates used:

A. NTSC MODE (URCLK=7.15909)

Required BAUD RATE	COUNT (HEX)	BAUD RATE obtained	Percent error, %
50	22F4	49.999	.0015
75	174D	74.999	.0015
110	0FE3	109.991	.008
134.5	0CFE	134.488	.009
150	0BA6	149.998	.0015
300	05D2	299.895	.035
600	02E9	599.79	.035
1200	0174	1199.58	.035

Required BAUD RATE	COUNT BAUD RATE (HEX)	obtained	Percent error, %
1800	00F8	1796.96	.17
2400	00B9	2393.74	.30
3600	007B	3508.41	.23
4800	005C	4811.22	.23
7200	003D	7216.82	.23
9600	002E	9520.07	.83
19200	0016	19454.00	1.323
56000	0007	55930.4	.124

B. PAL MODE (URCLK=7.09375 MHz)

Required BAUD RATE	COUNT BAUD RATE (HEX)	obtained	Percent error, %
50	22A2	50.001	0.002
75	1716	75.005	0.002
110	0FBE	109.987	0.01
134.5	0CDF	134.514	0.01
150	0B8B	149.986	0.009
300	05C5	299.937	0.009
600	02E2	599.945	0.009
1200	0170	1198.27	.144
1800	00F5	1802.27	.126
2400	00B8	2396.54	.144
3600	007A	3604.55	.126
4800	005B	4819.12	.398
7200	003D	7150.96	.68
9600	002D	9638.25	.4
192000	0016	19276.5	.4
56000	0007	55419.9	1.04

NOTE: Errors of less than 1.5% are acceptable

2.6.5 CHARACTER CONFIGURATION

P= PARITY BIT
STP= STOP BIT

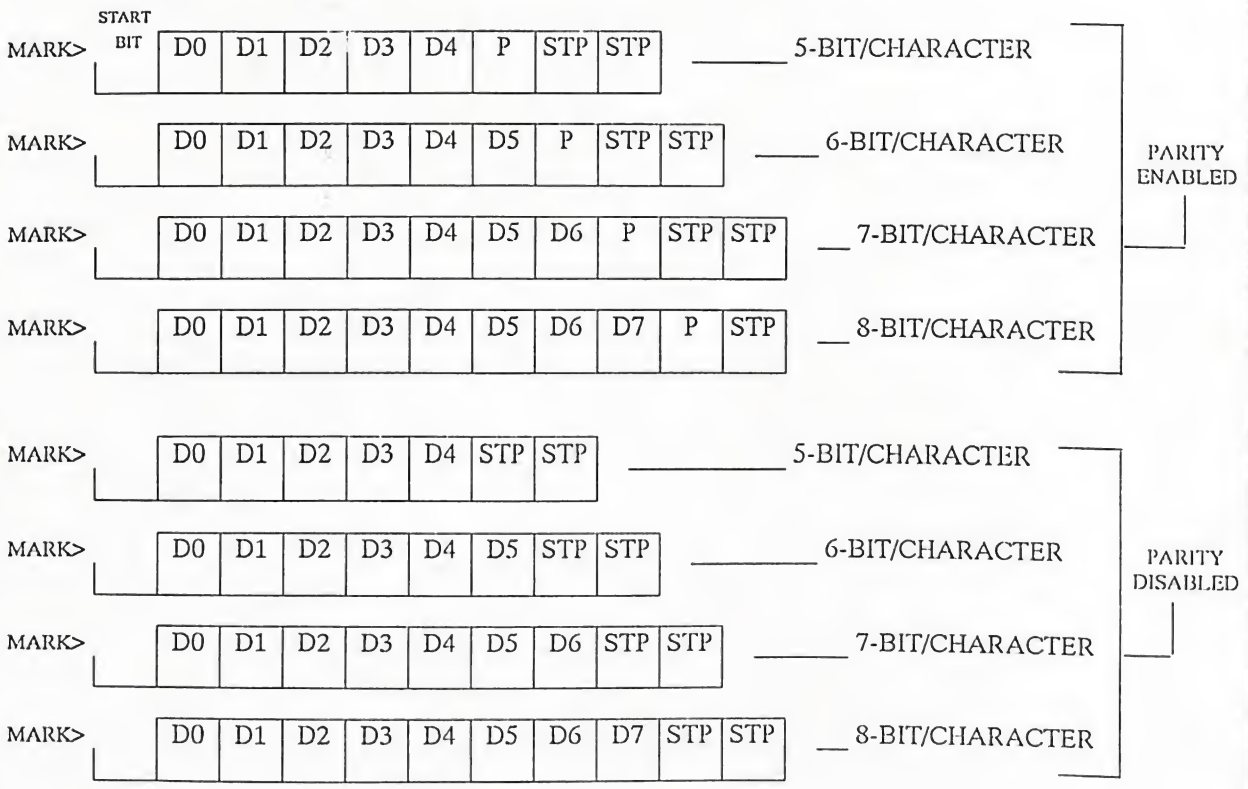

FIGURE 5
CHARACTER CONFIGURATION

			TITLE	
			IC, LSI, MICROPROCESSOR, 4510	
SIZE	DRAWING NUMBER	REV.	SCALE	SHEET 46 OF 52
A	390490	1		

4.0 ELECTRICAL REQUIREMENTS

4.1 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed may causepermanent damage to the circuit. Functional operation ofthe device at these or any conditions other than those indicatedin the operating conditions of this specification is not implied. Exposure to the maximum ratings for extended periods may adversely affect device reliability.

Characteristic	min	max	units
4.1.1 ambient temperature under bias	-25	+125	°C
4.1.2 storage temperature	-65	+150	°C
4.1.3 applied supply voltage	-0.5	+7.0	volts
4.1.4 applied output voltage	-0.5	+5.5	volts
4.1.5 applied input voltage	-2.0	+7.0	volts
4.1.6 power dissipation	-	1.5	watts

4.2 OPERATING CONDITIONS

All electrical characteristics are specified overr the entire range of the operating conditions unless specifically noted. All voltages are referenced to Vss = 0.0 V

	Condition	min	max	units
4.2.1	supply voltage (V_{cc})	4.75	5.25	volts
4.2.2	Free air temperature	0	70	°C

4.3 INTERFACE CHARACTERISTICS

	Characteristic	Symbols	min	max	units	Conditions
4.3.1	Input high level	V_{ih}	2.0	V_{cc}+1	volts	except RES/
			2.7	V_{cc}+1	volts	RES/ only
4.3.2	Input low level	V_{il}	-0.5	0.8	volts	
4.3.3	Output high level	V_{oh}	2.4	-	volts	I_{oh} = -400 ua
4.3.4	Output low level	V_{ol}	-	0.4	volts	I_{ol} = 3.2 ma
4.3.4A	Output low level (RESET/, EXTRST/)	V_{ol}	-	0.4	volts	I_{ol} = 3.2 ma
4.3.5	Input leakage	I_{in}	-10	10	uamps	0.0v<V_{in},V_{cc}
4.3.6	Output leakage	I_{lkg}	-10	10	uamps	0.4v<V_{out}<2.4v (Deselected)
4.3.7	Supply current	I_{cc}	-	200	mamps	Outputs open (V_{cc} = 5.25v)

4.4 SWITCHING CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
4.4.1 Ph0cycle time	t_{cyc}	279		ns
4.4.2 Baudclk cycle time	t_{c7mcyc}	140		ns
4.4.3 Baudclk width hi	t_{p7mh}	60		ns
4.4.4 Baudclk width lo	t_{p7ml}	60		ns
4.4.5 PH0 width hi	t_{pwh}	125		ns
4.4.6 PH0 width lo	t_{pwl}	125		ns
4.4.7 clocks, rise fall	t_{xr}, t_{xf}		15	ns
4.4.8 Address Setup	t_{ads}		80	ns
4.4.9 Address Hold	t_{adh}	15		ns
4.4.10 Datain Setup	t_{dis}	40		ns
4.4.11 Data in Hold	t_{doh}		90	ns
4.4.12 Data out Delay	t_{dod}	30		ns
4.4.13 Address to no I/O Delay	t_{anio}		10	ns
4.4.14 Port setup time	t_{ps}	60		ns
4.4.15 Port Output Delay	t_{pd}		250	ns
4.4.16 IRQ, NMI Setup	t_{cs}	30		ns
4.4.17 IRQ, NMI Hold	t_{ch}	25		ns
4.4.18 IRQ, NMI Output Delay	t_{pirq}		210	ns
4.4.19 PC2 output Delay	t_{ppc}		110	ns
4.4.20TXD Output Delay t_{ptxd}			110	ns
4.4.21 PRC2 Output Delay	t_{ptxd}		110	ns
4.4.22PRC2 width hi, lo	t_{urew} (min 2tc7mcyc)	280		ns
4.4.23 sp Setup	t_{scnt}	0		ns

Note:

FLAGa, FLAGB, CNTin, SPin are asynchronous inputs with respect to PH0 or BAUDCLK.
PRxx are the PRA, PRB, PRC, PRE, PRC46, PRC57 port pins.

5.0 APPLICATION NOTES

The following figure outlines the pin name re-assignment for implementation in the c65 computer

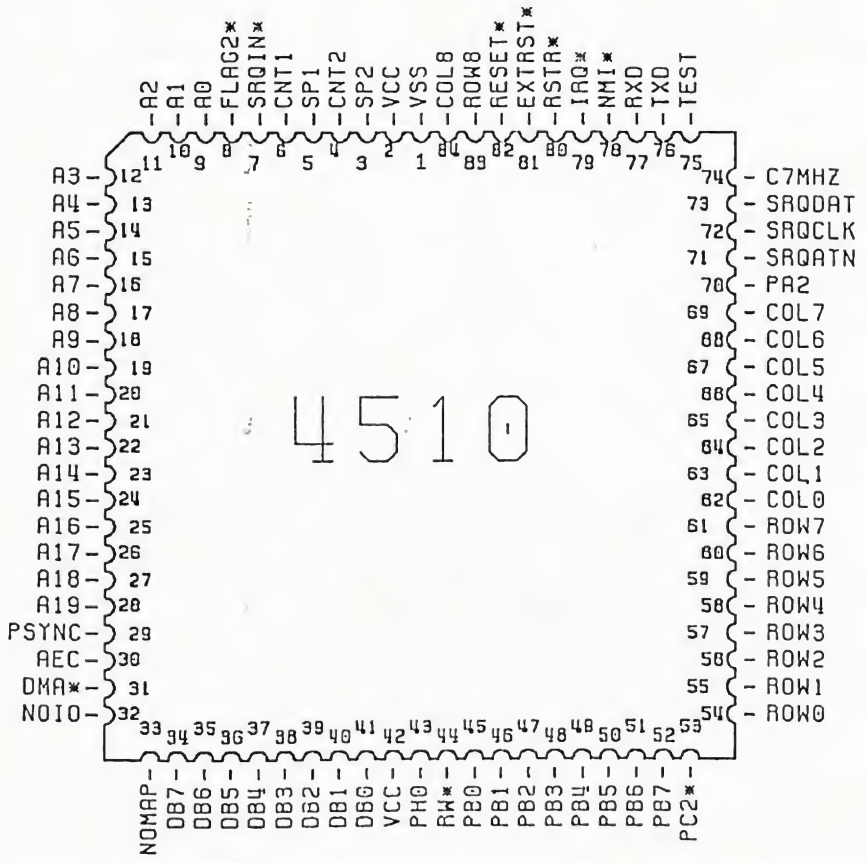

FIGURE 6
C65 PIN NAME REASSIGNMENT

			TITLE	
			IC, LSI, MICROPROCESSOR, 4510	
SIZE	DRAWING NUMBER	REV.	SCALE	SHEET 49 OF 52
A	390490	1		

6.0 PHYSICAL REQUIREMENTS

6.1 MARKING

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code. Pin No. 1 shall be identified.

6.2 PACKAGING

The interconnected logic circuitry shall be contained in a standard, plastic ZIP (Zig-Zag in-line package) Package with exterior dimensions per Figure 2.

7.0 ENVIRONMENTAL REQUIREMENTS

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request):

Operating Temperature	0 to 70 deg. C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85 deg. C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

7.1 PROCESS QUALIFICATION TESTS

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

7.2 ENVIRONMENTAL TEST CONDITIONS

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85 deg. C and 95% RH non-condensing) for 168 hours.

2. Operating life (1000 hours at 70 deg. C ambient temperature)

3. Solderability per MIL-STD-883, Method 2003

4. Pressure cooker (15 psig, 120 deg. C, and 100% RH for 24 hours)

5. Solvent resistance per MIL-STD-883,Method 2015, using water and trichloroethane

6. Solder temperature resistance (250 deg. C for five seconds)

7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

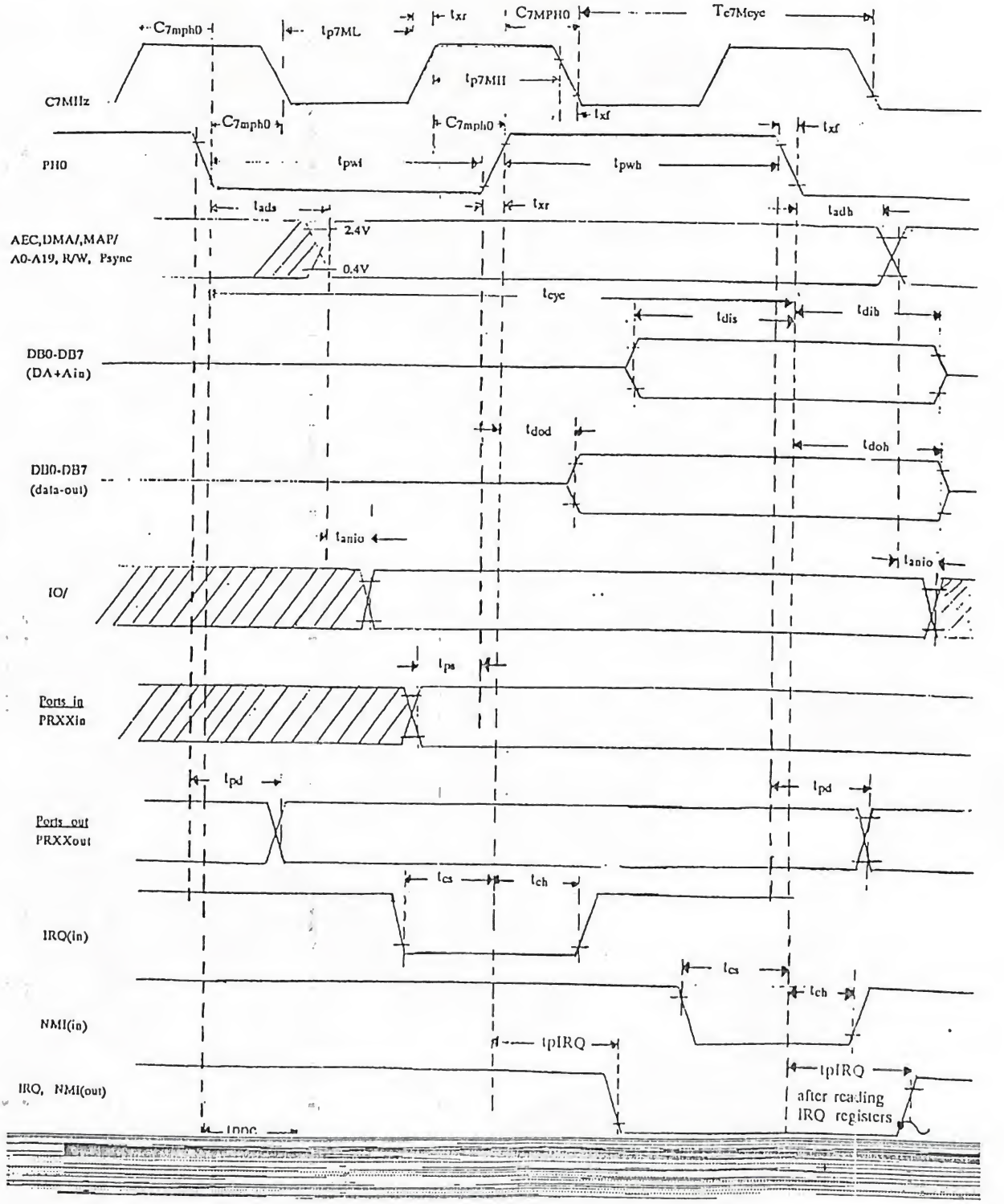

FIGURE 7 - 4510 TIMING

Commodore			TITLE: IC, LSI, MICROPROCESSOR, 4510	
SIZE: A	DRAWING NUMBER: 390490	REV.: 1	SCALE:	SHEET 51 OF 52

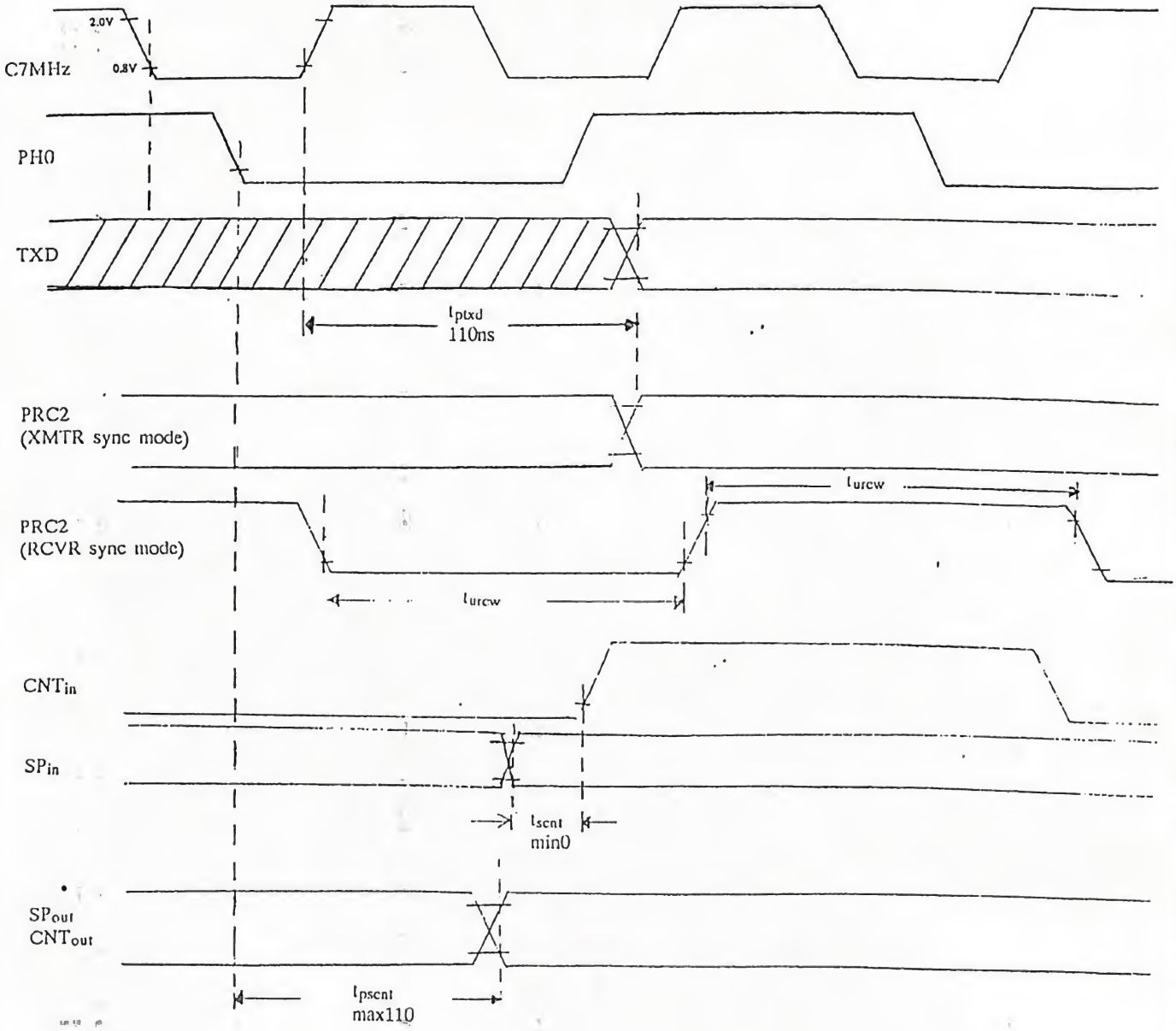

FIGURE 8 - 4510 TIMING (II)

Commodore			TITLE: IC, LSI, MICROPROCESSOR, 4510	
SIZE: A	DRAWING NUMBER: 390490	REV.: 1	SCALE:	SHEET 52 OF 52

APPROVED VENDOR LIST

Commodore Part Number	Vendor	Vendor Part Number
390490-01	CSG	4510 R4
390490-02	CSG	4510 R5

Commodore			TITLE: IC, LSI, MICROPROCESSOR, 4510	
SIZE	DRAWING NUMBER	REV.	SCALE	SHEET 1 OF 1
A	390490	1		